VXI

GPIB-VXI/C
User Manual

May 2002 Edition
Part Number 370556A-01

Worldwide Technical Support and Product Information

ni.com

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FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC Web site at `http://www.fcc.gov` for more information.

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Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

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Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

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* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

This manual contains information you need to use the GPIB-VXI/C in your VXIbus system. It describes the function and behavior of GPIB-VXI/C units configured with the standard user firmware option.

Conventions

The following conventions appear in this manual:

This icon denotes a note, which alerts you to important information.

This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

italic

Italic text denotes variables, emphasis, a cross reference, an introduction to a key concept, or Word Serial commands and queries. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace`

Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

`monospace italic`

Italic text in this font denotes text that is a placeholder for a word or value that you must supply.

`monospace bold`

Bold text in this font denotes the messages and responses that the computer automatically prints to the screen. This font also emphasizes lines of code that are different from the other examples.

`<hex value>`

Angle brackets enclosing a term in monospace denote a parameter.

Numbers in this manual are base 10 unless noted as follows:

- Binary numbers are indicated by a -b suffix (for example, 11010101b).
- Octal numbers are indicated by an -o suffix (for example, 325o).
- Hexadecimal numbers are indicated by an -h suffix (for example, D5h).
- ASCII character and string values are indicated by double quotation marks (for example, “This is a string”).

In this manual, the symbol <CR> is used to indicate the ASCII carriage return character. The symbol <LF> is used to indicate the ASCII linefeed character. The symbol <CRLF> is used to indicate a carriage return followed by a linefeed.

Terminology specific to a chapter or section is defined at its first occurrence.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *IEEE Standard Codes, Formats, Protocols, and Common Command*s, ANSI/IEEE Standard 488.2-1987
- *IEEE Standard Digital Interface for Programmable Instrumentatio*n, ANSI/IEEE Standard 488.1-1987
- *IEEE Standard for a Versatile Backplane Bus: VMEbu*s, ANSI/IEEE Standard 1014-1987
- *VXIbus Mainframe Extender Specificatio*n, VXI-6, Rev. 1.0, VXIbus Consortium
- *VXIbus System Specificatio*n, VXI-1, Rev. 1.3, VXIbus Consortium

1

General Description

This chapter contains a brief overview of the GPIB-VXI/C and its VXIbus and GPIB capabilities. This chapter also contains an overview of the local command set, an introduction to Code Instruments (CIs), and a description of the front panel.

Overview

The GPIB-VXI/C is a C-sized VXIbus module that links the industry-standard IEEE-488 (GPIB) bus and the VXIbus. The GPIB-VXI/C performs transparent conversion of the GPIB signals and protocols to VXIbus signals and protocols, so that a GPIB Controller can control VXIbus instruments in the same way that it controls GPIB instruments.

The GPIB-VXI/C is factory configured to function as the system Resource Manager (RM). It performs the VXIbus startup configuration, self-test, and initialization functions, as well as VXIbus Slot 0-related services. You can defeat the RM and Slot 0 functions individually so that the GPIB-VXI/C can coexist with another RM and/or be located in any slot.

What Your Kit Should Contain

Your GPIB-VXI/C kit contains a GPIB-VXI/C module and documentation. The GPIB-VXI/C part number and serial number are printed on the label affixed to its shield casing.

Optional Equipment

You can contact National Instruments to order any of the following cables:

- Type S5 serial port cable, 25-pin (2 m), part number 181138-02
- Type S6 serial port cable, 9-pin (2 m), part number 181139-02
- Type X2 double-shielded GPIB cables (0.5 m, 1 m, 2 m, 4 m, or 8 m), part numbers 763061-005, -01, -02, -03, and -04, respectively

Unpacking

Caution Your GPIB-VXI/C is shipped in an antistatic plastic bag to prevent electrostatic damage to components on the module. To avoid such damage while handling the module, touch the plastic bag to a metal part of your VXIbus mainframe chassis before removing the module from the bag.

Before removing the module from its plastic bag, verify that the pieces contained in the package you received match the kit parts list. Contact National Instruments if there are missing components.

Now remove the module from the bag and inspect the module for loose components or any other sign of damage. Notify National Instruments if the module appears damaged in any way. Do *not* install a damaged module into your VXIbus mainframe.

VXIbus Characteristics

The GPIB-VXI/C has the following VXIbus capabilities:

- Fully compatible with VXIbus System Specification
- VXIbus Resource Manager (RM) (defeatable)
- VXIbus Slot 0 support (defeatable)
- VXIbus Message-Based Commander and Message-Based Servant
- VXIbus master—A16, A24, D16, D08(EO)
- VXIbus slave—A16, A24, A32, D16, D08(EO)
- Up to 4 MB of dual-ported (shared) memory
- Three programmable VXIbus interrupt handlers
- IEEE 488.1 and IEEE 488.2-compatible multiple primary or multiple secondary 488-VXIbus translator

GPIB Characteristics

The GPIB-VXI/C has the following GPIB characteristics:

- Communication with VXIbus Message-Based devices
  - VXI logical addresses are mapped to GPIB addresses
  - Automatically configured at startup
  - Programmable

- Interface
  - TNT4882C ASIC coupled with DMA
  - Full, transparent support of individual status bytes for each GPIB address
  - Buffered operation decouples GPIB and VXIbus operation
  - Controller can address one VXIbus device to talk and one or more other VXIbus devices to listen
- IEEE 488.1 capabilities
  - SH1 (Source Handshake)
  - AH1 (Acceptor Handshake)
  - T5, TE5 (Talker, Extended Talker): multiple primary or multiple secondary addressing
  - L3, LE3 (Listener, Extended Listener): multiple primary or multiple secondary addressing
  - SR1 (Service Request)
  - DC1 (Device Clear)
  - DT1 (Device Trigger)
  - RL0 (Remote Local)
  - PP0 (Parallel Poll)
- IEEE 488.2-compatible 488-VXIbus translation

The IEEE 488.1 capabilities are supported for all VXIbus devices associated with GPIB addresses. The IEEE 488.2 compatibility applies to 488.2-compatible VXIbus devices associated with GPIB addresses through the GPIB-VXI/C.

Local Command Set Overview

The GPIB-VXI/C local command set supports the following types of operations:

- System configuration and control
  - Help
  - General configuration
  - RM information extraction
  - VXI-defined common ASCII system commands
  - Dynamic system configuration and reconfiguration

  - GPIB address configuration
  - VXIbus interrupt handler configuration
  - IEEE 488.2 common commands
- Instrument development and test
  - VXIbus access
  - Word Serial communication
- CI user and development
  - CI configuration

You can access the command set from the GPIB port, the serial port, and through Word Serial Protocol communication. You also can use separate programmable local command response modes for interactive and control program operation.

Code Instruments

The GPIB-VXI/C can run software modules called *Code Instruments* (CIs) that perform special functions in the VXIbus environment. The CIs supported by National Instruments provide the following:

- Optimized I/O through NI-VISA (the NI-VISA CI; refer to Appendix A, *Using the NI-VISA Code Instrument*, for more information)
- High-speed access to VXI memory and registers (the DMAmove CI; refer to Appendix B, *Using the DMAmove and CDS-852 Adapter Code Instruments*, for more information)
- Communication with Colorado Data Systems 73A-852 adapter modules (the CDS-852 CI; refer to Appendix B, *Using the DMAmove and CDS-852 Adapter Code Instruments*, for more information)

National Instruments does not support other CIs from legacy GPIB-VXI/C applications or development of new custom CIs.

Front Panel Features

The GPIB-VXI/C has the following front panel features:

- Five front panel LEDs
  - The *SYSFAIL* LED reflects the status of the backplane SYSFAIL* signal and indicates that a VXIbus device in the system has failed.
  - The *FAILED*, *TEST*, and *ON LINE* LEDs indicate the current GPIB-VXI/C status.
  - The *ACCESS* LED indicates when the GPIB-VXI/C is accessed from GPIB or VXIbus or when its MODID is asserted.
- Five front panel connectors
  - GPIB interface
  - Serial port
  - Trigger input
  - Trigger output
  - External CLK10 I/O
- Configurable reset pushbutton
  - Pushbutton resets backplane
  - Pushbutton resets GPIB-VXI/C
  - Pushbutton resets both backplane and GPIB-VXI/C

2

Configuration and Startup Procedures

This chapter contains information about the system configuration, GPIB-VXI/C configuration, and startup operation.

System Configuration

The typical system includes the following components:

- A VXIbus system mainframe containing the GPIB-VXI/C and instrument modules
- A host computer with a GPIB interface module and associated driver software (available for many computers from National Instruments) connected to the GPIB-VXI/C GPIB port
- A dumb terminal or host running a terminal emulator connected to the GPIB-VXI/C serial port (optional)

The serial port settings are 9,600 baud, 8-bit data, no parity, and one stop bit. Refer to Appendix D, *Connectors*, for descriptions of the RS-232 serial connector and the GPIB interface connector.

Cables for connecting the GPIB-VXI/C serial port to an RS-232 terminal or COM1 port on an IBM PC-compatible computer are available from National Instruments. Refer to the *Optional Equipment* section of Chapter 1, *General Description*, for more information.

GPIB-VXI/C Configuration

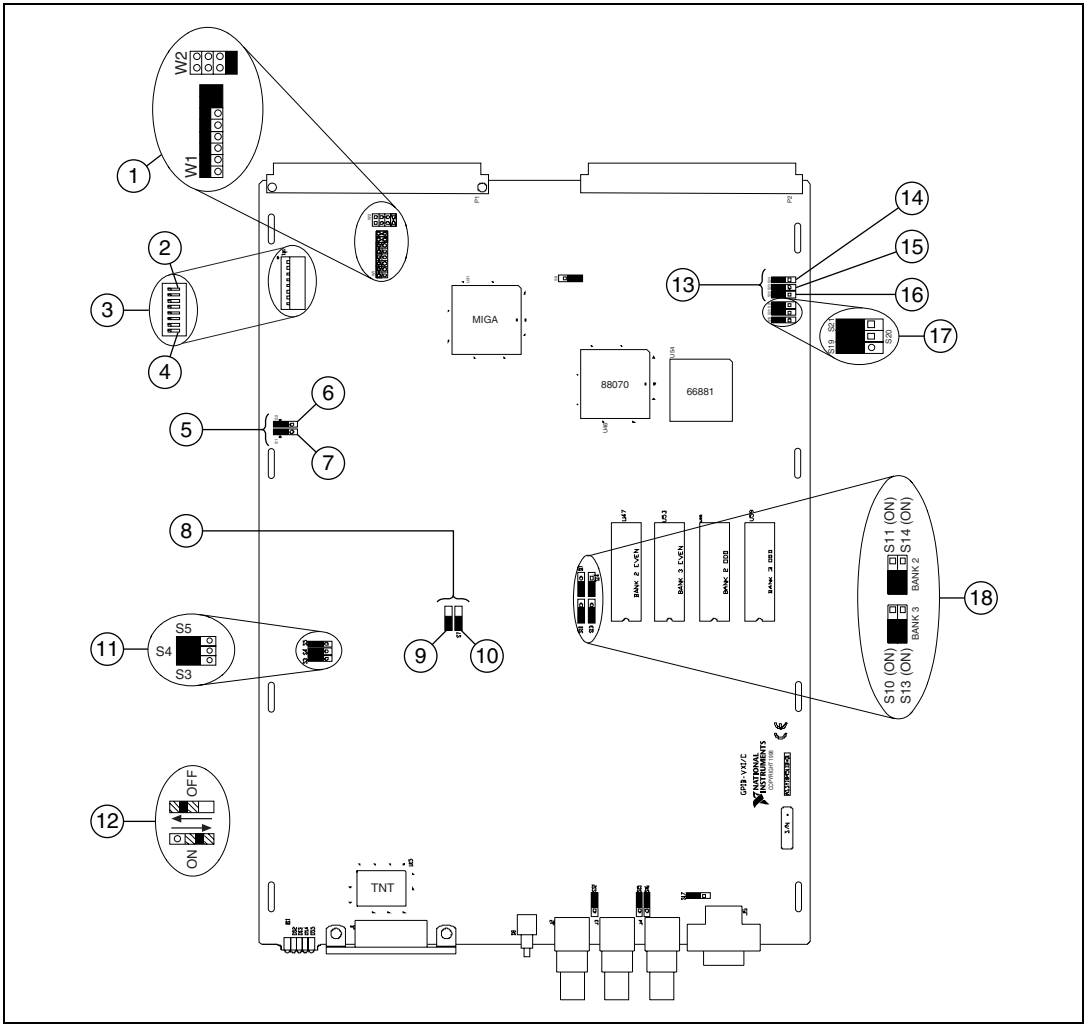
The GPIB-VXI/C factory configuration is shown in Table 2-1.

Table 2-1. GPIB-VXI/C Factory Configuration

Function	Factory Configuration
Startup Mode	488-VXI Runtime System Mode
VXIbus Characteristics Resource Manager (RM) Logical Address Servant Area Size Shared Memory Address Modifiers	 Enabled 0 0 0% of Installed Memory Supervisor A16, Supervisor A24 data
VXIbus Slot 0 Services CLK10 Driver CLK10 Source SYSCLK Driver Priority Arbiter Bus Timeout	 Enabled Onboard Clock Enabled Enabled Enabled (BTO ≥ 250 μsec)
Bus Requester	Level 3
VXI Interrupt Handlers	Unassigned
GPIB Addressing Mode	Multiple Secondary Addressing
GPIB-VXI/C GPIB Primary Address	1
Serial Port System Startup Messages Console Local Command Port Discrete Fault Indicator (DFI)	 Disabled Enabled Normally Open
Front Panel BNC Termination External Clock Input External Trigger Input	 Unterminated Unterminated

You do not have to change the GPIB-VXI/C factory configuration to use it as a Slot 0 Resource Manager. The following sections describe the factory configuration settings and present alternate configurations. Figure 2-1 shows the location of the GPIB-VXI/C configurable components and their physical location relative to some of the major circuit components. The jumpers and switches are represented in their factory default positions.

Note The GPIB-VXI/C is housed in a metal enclosure that has cutouts for access to all switches and jumpers associated with Slot 0/Non-Slot 0 settings, start-up mode, and Shared RAM settings. Under normal circumstances, you do not need to open the enclosure.



1	VXIbus Requester Level	7	S1 (OFF)	13	Slot 0 Switches
2	MSB	8	Installed RAM Switches	14	S24 (ON)
3	Logical Address DIP Switch (set to FFh)	9	S6	15	S23 (ON)
4	LSB5 Shared RAM Switches	10	S711Address Modifiers (ON)	16	S22 (ON)
5	S1, S2	11	S3, S4, S5	17	Startup Mode Switches (ON)
6	S2 (OFF)	12	Detail of Switch Settings	18	EPROM Expansion Switches

Figure 2-1. GPIB-VXI/C Parts Locator Diagram

Setting the Logical Address, GPIB Primary Address, and Servant Area Size

You can change the logical address, GPIB primary address, and Servant area size by running the nonvolatile memory configuration utility as described in the *Change Configuration Information* section of Chapter 4, *Nonvolatile Configuration*.

You can also change the logical address by setting DIP switch SW1. By default, all the switches are set to the Up position (0xFF). At this setting, the GPIB-VXI/C reads the logical address from the onboard EEPROM. To change the logical address, set the switches to the hex value of the logical address. Switch position 1 is the MSB; 8 is the LSB. Up is logical 1; down is logical 0.

Verifying the Installed RAM Size

The GPIB-VXI/C contains 4 MB of factory-installed local RAM but is configured to use the minimum amount of 512 KB. Table 2-2 lists the RAM configurations and their associated switch settings. You can use this information to change the board configuration.

Table 2-2. Installed RAM Configuration

Installed Memory Size	Switch S6 Setting	Switch S7 Setting
512 KB	OFF	OFF
1 MB	OFF	ON
2 MB	ON	OFF
4 MB	ON	ON

Table 2-3 shows the relationship between the amount of installed memory, the local address range occupied by the memory, and the range of VXI A24 addresses accessible by the GPIB-VXI/C as a bus master.

Table 2-3. GPIB-VXI/C CPU Local and A24 Memory Ranges

Installed Memory Size	Installed Memory Local Address Range		Accessible VXI A24 Address Range	
	Start	End	Start	End
512 KB	000000h	07FFFFh	080000h	E7FFFFh
1 MB	000000h	0FFFFFh	100000h	E7FFFFh
2 MB	000000h	1FFFFFh	200000h	E7FFFFh
4 MB	000000h	3FFFFFh	400000h	E7FFFFh

Setting the Shared Memory Size

You can set the amount of memory that is shared with the VXIbus by altering the settings of switches S1 and S2. Table 2-4 gives the S1 and S2 switch settings for sharing various portions of RAM with the VXIbus for each possible installed memory configuration.

Table 2-4. Shared Memory Switch Settings

Configured Memory Size	Amount of Installed Memory Shared with VXIbus			
	S1 ON S2 ON	S1 OFF S2 ON	S1 ON S2 OFF	S1 OF S2 OFF
512 KB	512 KB	256 KB	128 KB	none
1 MB	1 MB	512 KB	256 KB	none
2 MB	2 MB	1 KB	512 KB	none
4 MB	4 MB	2 MB	1 MB	none

Note The RAM shared with the VXIbus will be the upper portion of the installed memory.

The GPIB-VXI/C Offset Register holds the shared memory VXI A24 base address, as described in the VXIbus specification. The RM automatically configures the Offset Register at startup.

Setting the Reset Operation

The GPIB-VXI/C has three configurable reset parameters. They can be enabled or disabled and are as follows:

- Pushbutton resets backplane (asserts SYSRESET* signal).
- Pushbutton resets GPIB-VXI/C (asserts local reset signal).
- Backplane SYSRESET* signal resets GPIB-VXI/C (SYSRESET* on backplane asserts local reset).

The reset parameters can be altered by the nonvolatile memory configuration described in the *Change Configuration Information* section of Chapter 4, *Nonvolatile Configuration*.

Setting the VXIbus Requester Level

You can change the VXIbus requester level of the GPIB-VXI/C by moving the jumpers on jumper blocks W1 and W2 as shown in Figure 2-2. The GPIB-VXI/C is configured at the factory to be a Level 3 requester.

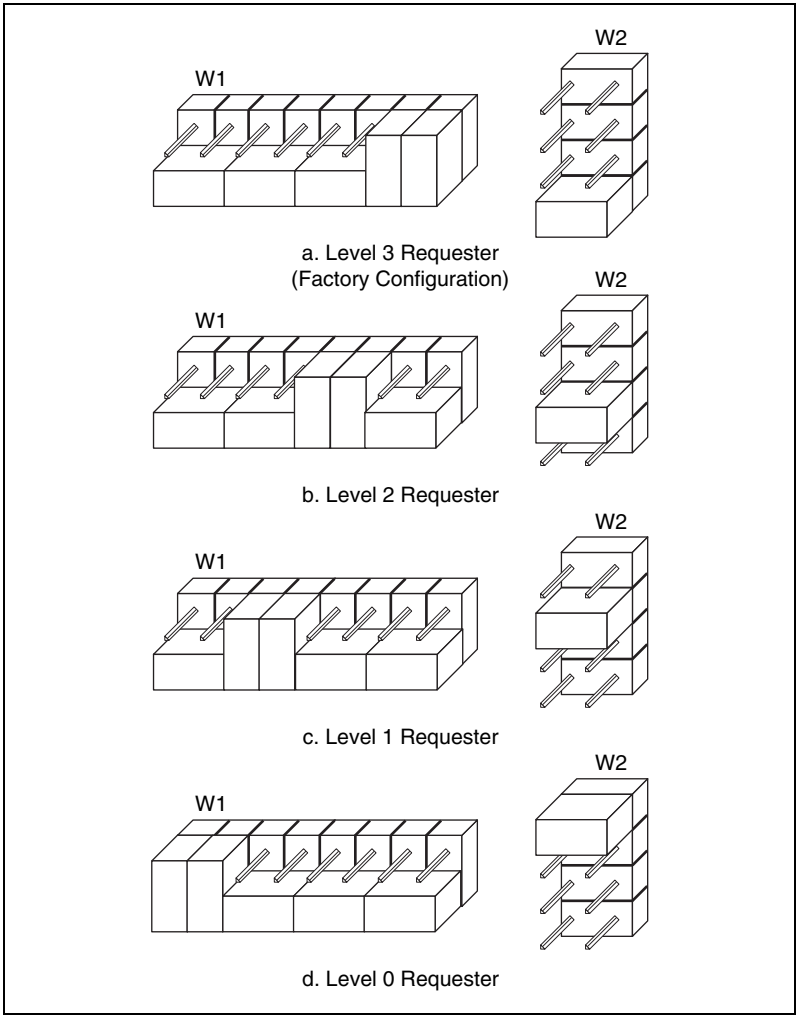


Figure 2-2. VXIbus Requester Jumper Settings

Setting the VXI Interrupt Handler Levels

As part of the hardware capabilities on the GPIB-VXI/C, there are three VXI programmable interrupt handlers. They can be assigned dynamically by the RM or statically according to the contents of the nonvolatile memory as described in Chapter 4, *Nonvolatile Configuration*.

External Input Termination

Switches S12 and S16 enable a 50-ohm termination to ground for the external trigger and external clock inputs, respectively. The GPIB-VXI/C is factory-configured with the termination disabled for both the external trigger and the external clock inputs. Figure 2-3 shows the settings required to enable or disable the termination on the external trigger. Figure 2-4 shows the settings required to enable or disable the termination on the external clock.

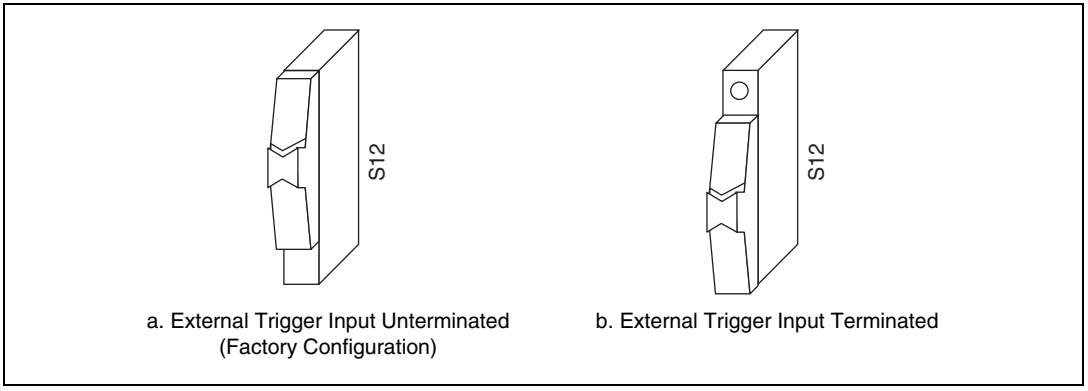


Figure 2-3. External Trigger Input Termination

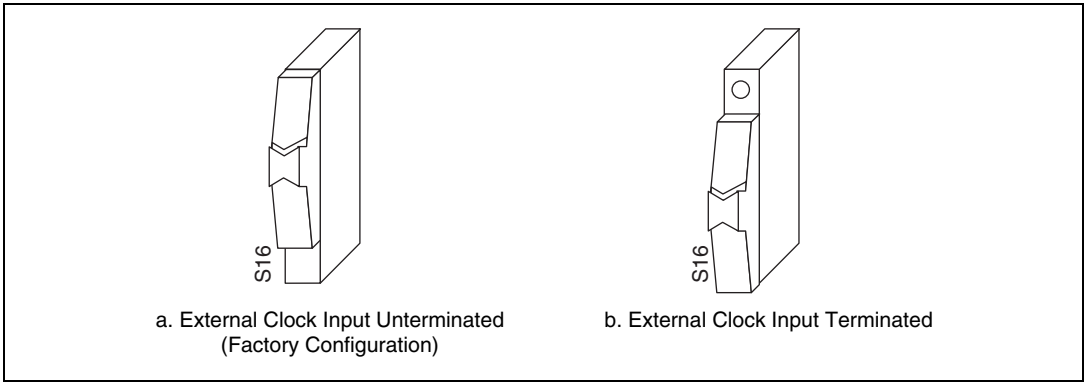


Figure 2-4. External Clock Input Termination

EPROM Configuration

The amount of read-only memory (ROM) in the GPIB-VXI/C can vary from 512 KB to 1 MB. The standard configuration consists of 512 KB of EPROM, which is used for the operating firmware. The GPIB-VXI/C also includes four sockets for EPROM expansion.

The EPROM expansion sockets accommodate combinations of 2764, 27128, 27256, 27512, and 27010 EPROMs. Table 2-5 lists the possible EPROM memory configurations. Bank 2 has a base address of E80000h and Bank 3 starts at EC0000h. The maximum EPROM expansion memory size is 512 KB.

Table 2-5. Expansion EPROM Configurations

EPROM Size	BANK 2 (U47, U55)	BANK 3 (U53, U59)	S11	S14	S10	S13	End Address
16 KB	2764	None	OFF	OFF	OFF	OFF	E83FFFh
32 KB	27128	None	OFF	OFF	OFF	OFF	E87FFFh
64 KB	27256	None	OFF	ON	OFF	OFF	E8FFFFh
128 KB	27512	None	ON	ON	OFF	OFF	E9FFFFh
256 KB	27010	None	ON	ON	OFF	OFF	EBFFFFh
272 KB	27010	2764	ON	ON	OFF	OFF	EC3FFFh
288 KB	27010	27128	ON	ON	OFF	OFF	EC7FFFh
320 KB	27010	27256	ON	ON	OFF	ON	ECFFFFh
384 KB	27010	27512	ON	ON	ON	ON	EDFFFFh
512 KB	27010	27010	ON	ON	ON	ON	EFFFFFh

When you insert EPROMs into the expansion EPROM slots, orient them according to the silkscreen printed on the board as shown in Figure 2-1. The 2764, 27128, 27256 and 27512 EPROMs have fewer pins than the expansion sockets. In these cases, align the bottom pins of the EPROM with the *bottom* pins of the socket, leaving the top pins open, as illustrated in Figure 2-5.

Caution Improper EPROM installation can result in damage to the EPROM, the GPIB-VXI/C, or both.

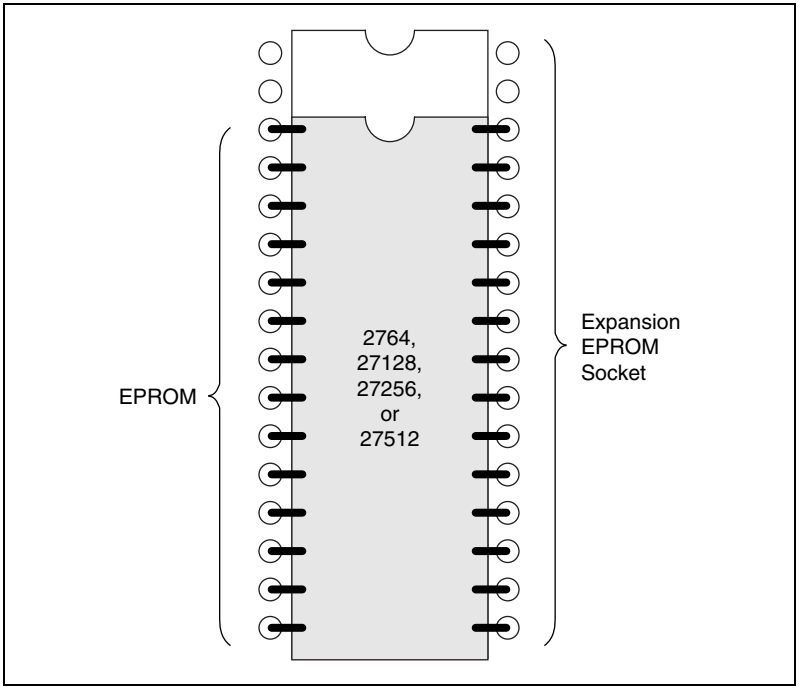


Figure 2-5. EPROM Insertion Position

Discrete Fault Indicator Configuration

The GPIB-VXI/C comes with a MATE-compatible Discrete Fault Indicator (DFI). The GPIB-VXI/C monitors the status of the VXIbus SYSFAIL* signal and relays the status to pins 1 and 6 of the RS-232 serial port. Refer to Appendix D, *Connectors*, for more information.

As shown in Figure 2-6 and Table 2-6, switch S17 determines the relationship between the SYSFAIL* signal and the serial port pins. If S17 is in the OFF position, the GPIB-VXI/C DFI is set to the normally open mode. Therefore, if SYSFAIL* is not asserted while the backplane is powered up, pins 1 and 6 will present an electrical open-circuit. In contrast, if the backplane is unpowered or SYSFAIL* is asserted, pins 1 and 6 will present an electrical short-circuit.

If S17 is in the ON position, the GPIB-VXI/C DFI is set to the normally closed mode. Therefore, if SYSFAIL* is not asserted while the backplane is powered-up, pins 1 and 6 will present an electrical short-circuit. In contrast, if the backplane is unpowered or SYSFAIL* is asserted, pins 1 and 6 will present an electrical open-circuit.

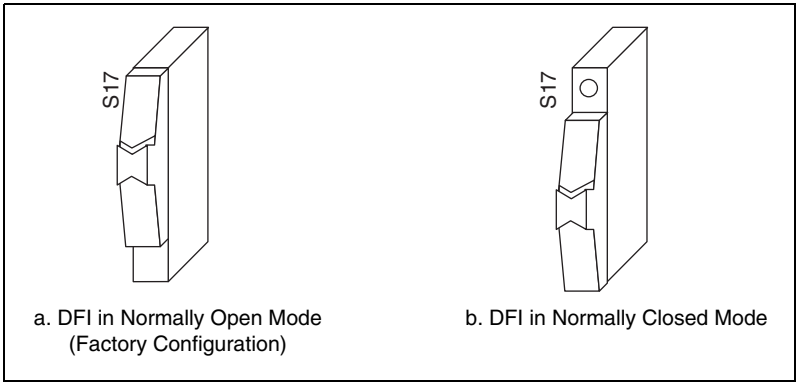


Figure 2-6. Discrete Fault Indicator Configuration

Table 2-6. Discrete Fault Indicator Options

Switch S17	Power	SYSFAIL	Pins 1 and 6
OFF Figure 2-6a	OFF ON ON	N/A Asserted Unasserted	Short-Circuit Short-Circuit Open-Circuit
ON Figure 2-6b	OFF ON ON	N/A Asserted Unasserted	Open-Circuit Open-Circuit Short-Circuit

Address Modifier Configuration

By setting onboard switches, you can have the GPIB-VXI/C specify the state of the VXIbus Address Modifiers during a VXI master access. During A16 accesses, the lines AM5, AM4, and AM3 are needed high, low, and high, respectively, and AM1 is needed low. During A24 accesses, the lines AM5, AM4, and AM3 are all needed high. The GPIB-VXI/C drives the upper three address modifier lines appropriately for every access. You should configure the GPIB-VXI/C to drive the lower three address modifier lines as needed.

Switches S3, S4, and S5 control the AM0, AM1, and AM2 signals. Figure 2-7 shows the valid settings of S3, S4, and S5.

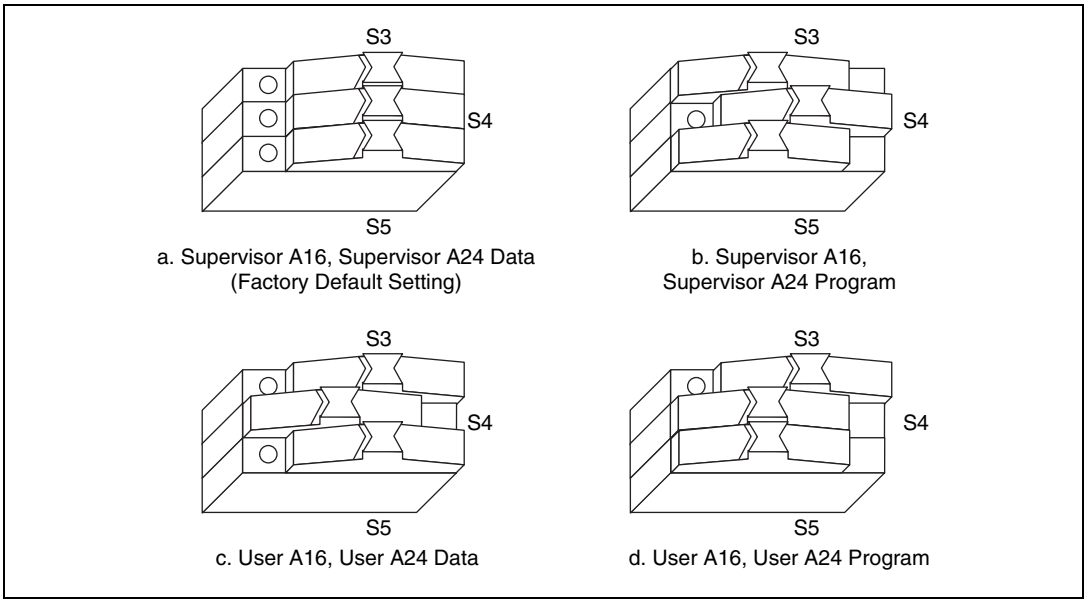


Figure 2-7. Address Modifier Signals Switch Settings

GPIB-VXI/C Startup Mode Configuration

Startup mode switches S19 and S20 control the GPIB-VXI/C operation mode at system startup. They select one of three modes, as shown in Figure 2-8. The three possible modes of startup are 488-VXI runtime system mode, nonvolatile configuration mode, and diagnostics mode.

- *488-VXI runtime system mode* is the startup mode for normal operation in a VXI system. The GPIB-VXI/C is configured at the factory to start up in this mode. The remainder of this chapter contains a description of operation in this mode.
- In *nonvolatile configuration mode*, you can edit the contents of the nonvolatile configuration parameter memory. Refer to Chapter 4, *Nonvolatile Configuration*, for more information on the nonvolatile configuration mode of the GPIB-VXI/C.
- In *diagnostics mode*, you can perform extensive offline diagnostic tests on the GPIB-VXI/C. Refer to Chapter 5, *Diagnostic Tests*, for a description of the GPIB-VXI/C self-tests.

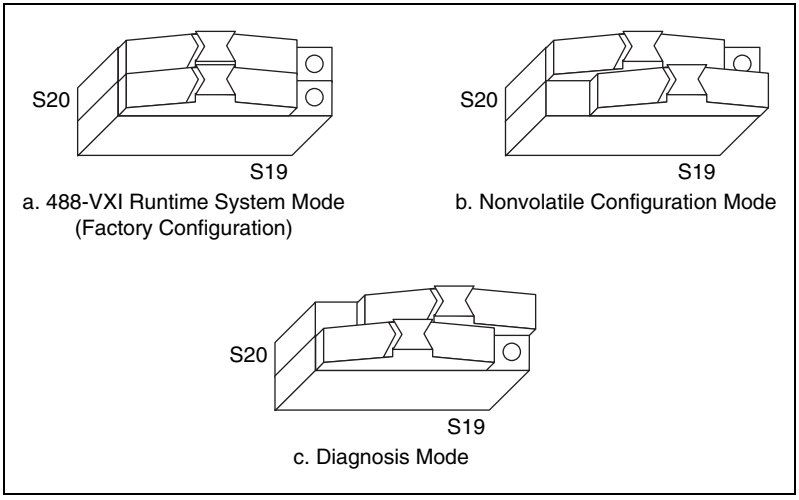


Figure 2-8. Startup Mode Switch Settings

488-VXI Runtime System Operation

The GPIB-VXI/C is factory configured as a Slot 0 Resource Manager. The Slot 0 and Resource Manager (RM) functions can be independently defeated, resulting in four modes of operation:

- Slot 0 Resource Manager (factory configuration)
- Non-Slot 0 Resource Manager
- Non-Slot 0 Message-Based device (non-Resource Manager)
- Slot 0 Message-Based device (non-Resource Manager)

This section describes the GPIB-VXI/C configuration procedures and startup behavior for each mode of operation.

Caution *Never* install a GPIB-VXI/C configured for Non-Slot 0 operation in Slot 0 or a GPIB-VXI/C configured for Slot 0 operation in any slot other than Slot 0. Doing so can damage the GPIB-VXI/C, the mainframe, or other modules.

System Startup Message Printing

The serial port startup printout enable switch S21 controls whether or not VXI system startup messages are printed to the serial port, as shown in Figure 2-9. The factory default configuration disables this function.

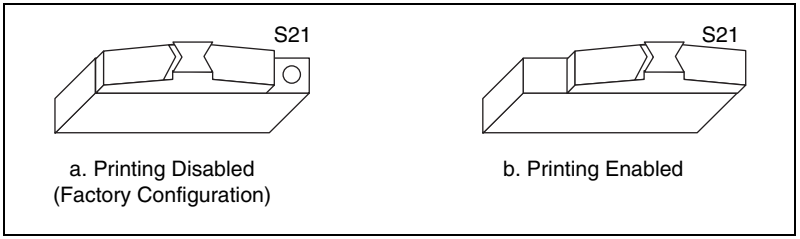


Figure 2-9. VXI System Startup Message Switch Settings

Slot 0 Resource Manager Configuration

You can configure the GPIB-VXI/C for Slot 0 Resource Manager operation by enabling the VXIbus Slot 0 functions and setting the logical address to 0, as shown in Table 2-7.

Table 2-7. Slot 0 Resource Manager Operation Switch and Jumper Settings

Jumper/Switch	Position	Function
Switches S9 and S15	Refer to Table 2-8.	CLK10 routing options.
Switch S22	ON	VXI BTO enabled.
Switch S23	ON	Bus arbiter and SYSCLK enabled. CLK10 sourcing for backplane is enabled.
Switch S24	ON	MODID pulled up.
Logical Address	Refer to Chapter 4, *Nonvolatile Configuration*.	Logical address is 0. Set in nonvolatile configuration or use the DIP switch.
Slot 0 Model Code	Refer to Chapter 4, *Nonvolatile Configuration*.	Model code is set to the Slot 0 value. Set in nonvolatile configuration.

Table 2-8. CLK10 Routing Options

Switch S15	Switch S59	Function
OFF	OFF	CLK10 sourced from onboard clock.
ON	OFF	CLK10 and EXT CLK connector sourced from onboard clock.
OFF	ON	CLK10 sourced from an external clock via the EXT CLK connector.
ON	ON	Invalid. Do not use this setting.

Slot 0 Resource Manager Operation

At startup, a GPIB-VXI/C configured as a Slot 0 Resource Manager performs its self-tests, executes the RM functions, and then enters its normal mode of operation.

Front Panel LED Indications for RM Operation

The five front panel LEDs are *SYSFAIL*, *FAILED*, *TEST*, *ON LINE*, and *ACCESS*. The GPIB-VXI/C uses the *FAILED*, *TEST*, and *ON LINE* LEDs to indicate the progress of its self-initialization, self-test, and RM functions. The LED indications are shown in Table 2-9. A successful system startup will sequence through the first five states. The point of failure is indicated for states in which the *FAILED* LED is lit for an extended period of time. The LED indications are identical for Slot 0 Resource Manager and Non-Slot 0 Resource Manager operation.

Table 2-9. Front Panel LED Indications for RM Operation

Sequence	FAILED	TEST	ON LINE	State	Point of Failure
1	OFF	OFF	OFF	No power	Failed before self-test
2	ON	OFF	OFF	In self-initialization	Failed in self-test
3	ON	ON	OFF	In self-test	—

Table 2-9. Front Panel LED Indications for RM Operation (Continued)

Sequence	FAILED	TEST	ON LINE	State	Point of Failure
4	OFF	ON	ON	Performing RM	—
5	OFF	OFF	ON	Online	—
	ON	ON	ON	Failed	Failed while in RM
	ON	OFF	ON	Failed	Failed while online
	OFF	ON	OFF	In nonvolatile configuration or diagnostics mode	—

The *SYSFAIL* LED is lit whenever any device in the system is asserting the VXIbus SYSFAIL* signal.

The *ACCESS* LED flashes whenever the GPIB-VXI/C is accessed from the GPIB or from the VXIbus. It also indicates when its MODID is asserted.

Self-Test Operation

The self-test sequence tests the basic functionality of many GPIB-VXI/C components, including EPROM, RAM, I^2C bus, RS-232 port, DMA channels, GPIB port, interrupt logic, timer, and VXIbus registers (MIGA). You can execute full tests of the GPIB-VXI/C in diagnostics mode, as described in Chapter 5, *Diagnostic Tests*.

RM Operation

The RM waits until all devices have stopped driving the VXIbus SYSFAIL* signal, or until five seconds have elapsed after the VXIbus SYSRESET* signal is negated. During this period, all of the VXIbus devices in the system should have completed their self-tests.

Note You can configure the GPIB-VXI/C to wait for any number of seconds before RM operations begin.

The RM then scans Logical Addresses 1 through 254 for *static configuration devices* (*SC devices*). For each SC device found, it reads the device class and manufacturer's ID code from the ID Register and the model code from the Device Type Register. If the device is an extended device, the RM reads its Subclass Register. The RM then performs slot associations for each static configuration device by reading its Status Register while asserting each MODID line.

The RM then looks for *dynamic configuration devices* (*DC devices*) at Logical Address 255 by asserting each MODID line and reading the device's ID Register. DC devices initially have a logical address of 255. The RM subsequently assigns each DC device a different logical address. For each DC device found, it not only reads the device's configuration registers as with SC devices, but also assigns each device the next unused logical address by writing the appropriate value to the device's Logical Address Register. Using the nonvolatile configuration mode, you can set the starting logical address for the RM to begin assigning DC devices. Refer to Chapter 4, *Nonvolatile Configuration*, for more information on nonvolatile configuration.

If any device has not passed its self-test, the RM forces that device offline by setting the Sysfail Inhibit and Reset bits in that device's Control Register.

The RM then determines the address space of each device by reading its ID Register. If the device's address space is A16/A24 or A16/A32, the RM allocates a section of A24 or A32 memory space to the device according to the memory requirements indicated by the contents of its Device Type Register and writes an appropriate value to the device's Offset Register.

The RM configures the initial Commander/Servant hierarchy according to each Commander's Servant area size, using the algorithm described in the VXIbus specification. The RM issues the appropriate *Read Servant Area* and *Device Grant* commands to each SC Commander. The RM retains all devices not assigned to other Commanders as its immediate Servants. Regardless of where DC device logical addresses are assigned, they are never granted to an SC Commander. The DC Commander/Servant hierarchy can be created in one of two ways:

- All DC devices can be automatically assigned as Servants of Logical Address 0 (the Resource Manager).
- A custom hierarchy can be created through the use of the local command set functions, as described in the *Dynamic Configuration Commands and Queries* section of Chapter 3, *Local Command Set*.

The RM then sends the *Read Protocols* query to all Message-Based devices. The response to the query is saved internally for later use in interrupt handler and GPIB configuration.

The RM configures the VXI interrupter and interrupt handlers using a seven-entry table contained in nonvolatile configurations. During the VXI interrupt configuration, the RM assigns interrupt levels to all Programmable Handlers (PH) and Programmable Interrupters (PI).

Each entry in the table represents the logical address of the handler that handles the corresponding level—1 through 7. If the handler is static, PI Servants are assigned to the level. If the device is a PH device, the RM assigns both it and any PI Servants to the corresponding level. Notice that if the table entry is FFh, the level is free to be assigned to any PH device. If only PH and PI devices are in a system, all entries may contain FFh. Refer to Chapter 4, *Nonvolatile Configuration*, for more information.

The remainder of the RM procedure depends upon whether the RM found any DC devices in the system.

Static Configuration Operation

When all of the previous operations are complete and successful, the RM sends the Word Serial command *Identify Commander* to all immediate Message-Based Servants with bus master capability. At this point, the RM is ready to bring the system into the Normal Operation sub-state. This is accomplished by sending the Word Serial query *Begin Normal Operation* to all top-level Commanders and immediate Message-Based Servants.

Dynamic Configuration Operation

If the system is a DC system (meaning that at least one DC device was found), and the nonvolatile configuration specifies that the RM should create a hierarchy with DC devices assigned to Logical Address 0, the RM follows the same steps as previously described in the Static Configuration Operation section. DC devices are treated as SC devices from this point on.

However, if you want to customize your own DC hierarchy and the nonvolatile configuration specifies that the RM not finish configuring the hierarchy, the GPIB-VXI/C RM does not send *Identify Commander* or *Begin Normal Operation* to any devices, either static or dynamic. The outside controller can then create the DC Commander/Servant hierarchy without having to dynamically reconfigure the system. Use the GPIB-VXI/C local command `DCGrantDev` to create the DC hierarchy. When the system is configured and ready to make a transition to the Normal Operation sub-state, send the GPIB-VXI/C local command `DCBNOSend`. `DCBNOSend` sends the *Identify Commander* and *Begin Normal Operation* commands to Message-Based devices as previously described in the *Static Configuration Operation* section. Refer to the *Dynamic Configuration Commands and Queries* section of Chapter 3, *Local Command Set*, for more information about dynamic configuration operation.

The GPIB-VXI/C then performs general configuration operations. The GPIB-VXI/C creates GPIB address links for its immediate Message-Based

SC Servants. After this, the GPIB-VXI/C RM and general configuration operations are complete.

GPIB Address Assignment

The GPIB-VXI/C automatically assigns GPIB addresses—primary or secondary—to itself and to each of its immediate Message-Based SC Servants. If the Message-Based device does not support minimal Word Serial[I] or VXIbus 488.2[I4] capabilities, no GPIB address link is created. The GPIB-VXI/C assigns a GPIB address to each device according to the top five bits of its logical address. For example, the GPIB address of a device with Logical Address 96 (01100000b) would be 12 (01100b).

If two or more devices have logical addresses with the same top five bits, the GPIB-VXI/C assigns GPIB addresses to devices in order of the least significant three bits. Conflicting devices are given the next available GPIB address. For example, if the GPIB-VXI/C and its Message-Based Servants have Logical Addresses 0, 24, 27, and 33, the GPIB-VXI/C assigns GPIB addresses as shown in Table 2-10.

Table 2-10. Example GPIB Address Assignment

Logical Address		3 LSB (Order of Assignment)	5 MSB	GPIB Address
Decimal	**Binary**	**Binary**	**Binary**	**Decimal**
0	00000000b	000b	00000b	0
24	00011000b	000b	00011b	3
33	00100001b	001b	00100b	4
27	00011011b	011b	00011b	5

In the example shown in Table 2-10, the device at Logical Address 27 was assigned GPIB Address 5 because addresses 3 and 4 were previously assigned. By spacing the GPIB-VXI/C Message-Based Servants at intervals of eight logical address locations you can avoid situations in which removing or adding one device changes the GPIB address of another device.

The default configuration for the GPIB-VXI/C is to use multiple GPIB secondary addresses (not multiple primary addresses). You can change the configuration to use multiple primary addresses through nonvolatile memory configuration as described in the *Change Configuration Information* section of Chapter 4, *Nonvolatile Configuration*.

You can change the self-assigned default GPIB address of the GPIB-VXI/C through the nonvolatile memory configuration as described in the *Change Configuration Information* section of Chapter 4, *Nonvolatile Configuration*. The default GPIB address of the GPIB-VXI/C when configured for multiple secondary addresses is Secondary Address 0 (Primary Address 1). The default GPIB address of the GPIB-VXI/C, when configured for multiple primary addresses, is Primary Address 1 (no secondary address).

At times, especially when using multiple primary addressing, you may find it necessary to avoid particular GPIB addresses to avoid conflicts with GPIB instruments outside of the VXI mainframe. You can specify what GPIB addresses to avoid through the nonvolatile memory configuration as described in the *Change Configuration Information* section of Chapter 4, *Nonvolatile Configuration*.

System Configuration Table

During the execution of the RM and general configuration operations, the GPIB-VXI/C builds up a table of system configuration information. Each device has an entry in the table containing the device's logical address, its Commander's logical address, its GPIB address, slot number, device class, manufacturer ID number, model code, memory space requirement, memory base address, and memory size. The GPIB-VXI/C retains this table after the RM and general configuration operations are complete. The information in the table is accessible through the GPIB-VXI/C local command set. The GPIB address entry is meaningful only for immediate Message-Based Servants of the GPIB-VXI/C.

Non-Slot 0 Resource Manager Configuration

Follow these steps to configure the GPIB-VXI/C for Non-Slot 0 Resource Manager operation. Refer to Table 2-11 for the switch and jumper settings.

1. Disable the VXIbus Slot 0 hardware functions.
2. Set the model code of the GPIB-VXI/C to be configured for Non-Slot 0 operation using the nonvolatile configuration mode.
3. Set the logical address to 0 in nonvolatile configuration mode or by using DIP switch SW1.

Table 2-11. Non-Slot 0 Resource Manager Operation Switch and Jumper Settings

Jumper/Switch	Position	Function
Switch S15	OFF	If S5 is ON, the GPIB-VXI/C also routes CLK10 to the EXT CLK connector on the front panel.
Switch S22	OFF	VXI BTO disabled.
Switch S23	OFF	Bus arbiter and SYSCLK disabled. CLK10 receiving from backplane.
Switch S24	OFF	MODID pulled down.
Logical Address	Refer to Chapter 4, *Nonvolatile Configuration*.	Logical address is 0. Set in nonvolatile configuration or use the DIP switch.
Non-Slot 0 Model Code	Refer to Chapter 4, *Nonvolatile Configuration*.	Model code is set to the Non-Slot 0 value. Set in nonvolatile configuration.

Non-Slot 0 Resource Manager Operation

The startup sequence for a GPIB-VXI/C configured for Non-Slot 0 Resource Manager operation is nearly identical to the Slot 0 Resource Manager operation; however, the GPIB-VXI/C controls the Slot 0 resources remotely in Non-Slot 0 RM operation.

A VXIbus Slot 0 device must be in the system. It must be either a Register-Based device that implements the MODID Register or a Message-Based device that supports the Word Serial commands *Read MODID*, *Set Lower MODID*, and *Set Upper MODID*. VXIbus Specification Revision 1.2 Message-Based Slot 0 devices are not supported.

Non-Slot 0 Message-Based Device Configuration (Non-Resource Manager)

Follow these steps to configure the GPIB-VXI/C for Non-Slot 0 Message-Based operation. Refer to Table 2-12.

1. Disable the VXIbus Slot 0 functions.
2. Set the model code of the GPIB-VXI/C to be configured for Non-Slot 0 operation using the nonvolatile configuration mode.
3. Set the logical address to a non-zero value with an appropriate Servant area size using the nonvolatile configuration mode or by using DIP switch SW1.

If the logical address is set to FFh in nonvolatile configuration (the DIP switch cannot set the logical address to FFh), the GPIB-VXI/C will participate in dynamic configuration. Otherwise, the GPIB-VXI/C is a static configuration device.

Table 2-12. Non-Slot 0 Message-Based Device Operation Switch and Jumper Settings

Jumper/Switch	Position	Function
Switch S15	OFF	If S5 is ON, the GPIB-VXI/C sources CLK10 at the front panel EXT CLK connector.
Switch S22	OFF	VXI BTO disabled.
Switch S23	OFF	Bus arbiter and SYSCLK disabled. CLK10 receiving from backplane.
Switch S24	OFF	MODID pulled down.
Logical Address	Refer to Chapter 4, *Nonvolatile Configuration*.	Logical address is not equal to 0. Set in nonvolatile configuration or by using DIP switch SW1.
Non-Slot 0 Model Code	Refer to Chapter 4, *Nonvolatile Configuration*.	Model code is set to the Non-Slot 0 value. Set in nonvolatile configuration.
Servant Area Size	Refer to Chapter 4, *Nonvolatile Configuration*	Set appropriate Servant area size. Set in nonvolatile configuration.

Non-Slot 0 Message-Based Device Operation

At startup, a GPIB-VXI/C configured as a Non-Slot 0 Message-Based device performs its self-tests. It then waits until it receives its *Device Grant* and *Begin Normal Operation* Word Serial commands. The RM grants any logical addresses to the GPIB-VXI/C that reside within its Servant area. When it responds to the *Begin Normal Operation* command, the GPIB-VXI/C enters its normal mode of operation.

Front Panel LED Indications for Message-Based Device Operation

The GPIB-VXI/C indicates the progress of its self-test with the *FAILED*, *TEST*, and *ON LINE* LEDs. The LED indications are shown in Table 2-13. A successful system startup sequences through the first five states. The point of failure is indicated for states in which the *FAILED* LED is

lit for an extended period of time. The LED indications are identical for Non-Slot 0 Message-Based device and Slot 0 Message-Based device operation.

Table 2-13. Front Panel LED Indications for Message-Based Device Operation

Sequence	FAILED	TEST	ON LINE	State	Point of Failure
1	OFF	OFF	OFF	No power	Failed before self-test
2	ON	OFF	OFF	In self-initialization	Failed in self-test
3	ON	ON	OFF	In self-test	—
4	OFF	ON	ON	Performing RM	—
5	OFF	OFF	ON	Online	—
	ON	OFF	ON	Failed	Failed while online
	OFF	ON	OFF	In nonvolatile configuration or diagnostics mode	—

Slot 0 Message-Based Device Configuration

Follow these steps to configure the GPIB-VXI/C for Slot 0 Message-Based operation. Refer to Table 2-14.

1. Enable the VXIbus Slot 0 functions.
2. Set the model code of the GPIB-VXI/C to be configured for Slot 0 operation using the nonvolatile configuration mode.
3. Set the logical address to a non-zero value with an appropriate Servant area size.

   If the logical address is set to FFh in nonvolatile configuration (the DIP switch cannot set the logical address to FFh), the GPIB-VXI/C will participate in dynamic configuration. Otherwise, the GPIB-VXI/C is a static configuration device.

Table 2-14. Slot 0 Message-Based Device Operation Switch and Jumper Settings

Jumper/Switch	Position	Function
Switches S9 and S15	Refer to Table 2-15.	CLK10 routing options.
Switch S22	ON	VXI BTO enabled.

Table 2-14. Slot 0 Message-Based Device Operation Switch and Jumper Settings (Continued)

Jumper/Switch	Position	Function
Switch S23	ON	Bus arbiter and SYSCLK enabled. CLK10 sourcing backplane.
Switch S24	ON	MODID pulled up.
Logical Address	Refer to Chapter 4, *Nonvolatile Configuration*.	Logical address is not equal to 0. Set in nonvolatile configuration or by using DIP switch SW1.
Slot 0 Model Code	Refer to Chapter 4, *Nonvolatile Configuration*.	Model code is set to the Slot 0 value. Set in nonvolatile configuration.
Servant Area Size	Refer to Chapter 4, *Nonvolatile Configuration*.	Set appropriate Servant area size. Set in nonvolatile configuration.

Table 2-15. CLK10 Routing Options

Switch S9	Switch S15	Function
OFF	OFF	CLK10 sourced from onboard clock.
OFF	ON	CLK10 and EXT CLK connector sourced from onboard clock.
ON	OFF	CLK10 sourced from an external clock via the EXT CLK connector.
ON	ON	Invalid. Do not use this setting.

Slot 0 Message-Based Device Operation

At startup, a GPIB-VXI/C configured as a Slot 0 Message-Based device performs its self-tests. It then waits until it receives its *Device Grant* (if any) and *Begin Normal Operation* Word Serial commands. The RM grants any logical addresses to the GPIB-VXI/C that reside within its Servant area. When the GPIB-VXI/C responds to the *Begin Normal Operation* command, it enters the normal mode of operation.

After the GPIB-VXI/C Passed bit is set, the RM can manipulate or read the MODID lines by sending the Word Serial queries *Read MODID*, *Set Lower MODID*, or *Set Upper MODID* to the GPIB-VXI/C.

3

Local Command Set

This chapter contains descriptions of the GPIB-VXI/C local command set. The descriptions of the commands and queries include syntax, format, and error handling information, as well as examples of the use of the commands and queries. The local command set supports the following types of operations:

- System configuration and control
  - Help
  - General configuration
  - Resource Manager (RM) information extraction
  - Dynamic system configuration and reconfiguration
  - VXI-defined Common ASCII System Commands
  - GPIB address configuration
  - VXIbus interrupt handler configuration
  - IEEE-488.2 common commands
- Instrument development and test
  - VXIbus access
  - VXI TTL/ECL trigger access
  - Word Serial communication

Note National Instruments no longer supports Code Instrument (CI) development. For more information about CI use and development, see the KnowledgeBase link at `ni.com/documents`.

The GPIB-VXI/C command set consists of commands and queries. Commands cause the GPIB-VXI/C to take some action. A query may also cause the GPIB-VXI/C to take some action, but it also returns a response containing data or other information.

Command Set Access

You can execute the local commands from the following ports:

- RS-232
- GPIB
- VXI Word Serial Communication

All ports are active when the GPIB-VXI/C is in the Normal Operation substate and operate independently of one another. The GPIB-VXI/C returns query responses only to the port originating the query. The GPIB-VXI/C also maintains a separate status state for each port.

You can use local commands to disable and re-enable each port's access to the local command set. The RS-232 port prompts you to enter a local command with the `GPIB-VXI>` prompt.

Command Syntax

The local command set parser is syntactically compatible with the IEEE-488.2 standard. It will accept numeric parameters in the 488.2 binary, octal, decimal, or hexadecimal formats. 488.2 binary parameters are prefixed with *#b*. Octal parameters are prefixed with *#q*, and hexadecimal parameters are prefixed with *#h*. Table 3-1 lists the most common numeric parameter types. The ranges given in Table 3-1 apply unless otherwise specified.

Table 3-1. Valid Ranges for Common Numeric Command Parameters

Parameter	488.2 Decimal	488.2 Hexadecimal
`<logical address>`	0 to 254	#h0 to #hFE
`<GPIB address>`	0 to 30	#h0 to #h1E
`<handler>`	1 to 3	#h1 to #h3
`<level>`	0 to 7	#h0 to #h7
`<A16 address>`	0 to 65,535	#h0 to #hFFFF
`<A24 address>`	2,097,152 to 14,680,062	#h200000 to #hE7FFFE
`<word value>`	0 to 65,535	#h0 to #hFFFF
`<byte value>`	0 to 255	#h0 to #hFF
`<Boolean>`	0 or 1	#h0 or #h1

The logical value of a `<Boolean>` parameter is FALSE for the numeric value 0 and TRUE for the numeric value 1.

The first parameter is delimited from the command name by a space ( ). Additional parameters are delimited from one another by a comma (,). The command names are not case sensitive.

In the command descriptions, parameters are enclosed in angle brackets (<>), and optional parameters are also enclosed in square brackets ([]). Do not enter the brackets as part of the command.

Multiple commands may be concatenated in a single command line if they are separated with semicolons (for example, `OBRAM?; DPRAM?`<CR>).

Command Line Termination

The serial port command line termination is a carriage return, shown in the subsequent function descriptions as <CR> (ASCII 0Dh). If the command contains a trailing linefeed, shown in the subsequent function descriptions as <LF> (ASCII 0Ah), it is ignored. The GPIB termination is EOI. Commands issued to the GPIB-VXI/C via VXI Word Serial Protocol are terminated by setting the END bit in the last *Byte Available* command. Responses are terminated by setting the END bit in response to the last *Byte Request* query.

Command and Query Responses

The local commands and queries have two response formats: *program* mode and *console* mode. Program mode responses have a terse data-only format that is intended for a control program to read and parse. Console responses are returned in the form of readable sentences, which are better suited for interactive command entry.

You can enable or disable each mode independently, except that one response mode must be enabled at all times. If both modes are simultaneously enabled, the program response is returned first, followed by the console response. The local commands used to control the response modes are `ProgMode` and `ConsMode`.

The response mode configuration is independent for each command source. Table 3-2 lists the default (startup/reset) response mode configurations.

Table 3-2. Default Response Mode Configurations

Port	Response Mode
RS-232	Console mode enabled, program mode disabled
GPIB	Program mode enabled, console mode disabled
VXI Word Serial	Program mode enabled, console mode disabled
Individual Code Instruments	Program mode enabled, console mode disabled

Command Response Format

Commands do not have program mode responses. They do not return a response to a port configured for console mode response only, unless the GPIB-VXI/C detects an error condition.

Console mode command responses are self-explanatory and are not described in this manual.

Query Response Format

Queries have both program and console mode responses. Program mode query responses are fixed-field formatted, with commas delimiting the fields. For example, the list of logical addresses returned by the `Laddrs?` query is returned as groups of three characters (to allow the field to accommodate the valid range of 0 to 254) separated by commas. The values are right-justified and padded with the ASCII space character ( ) (20h). For example, Logical Address 45 would be returned as (`45`). Unless otherwise noted, all returned values are decimal.

Console mode query responses are self-explanatory and are not described in this manual.

The query response line termination sequence, shown in the query descriptions as <CRLF>, indicates an ASCII 0Dh followed by 0Ah.

Error Reporting

Command syntax and execution errors are reported to the port where the command originated. If the program response mode is enabled, the GPIB-VXI/C returns an error message in the following format:

`$ <error code>`<CRLF>

The distinguishing characteristic of a program mode error message is the leading dollar sign character (`$`). A list of error code descriptions is given in Appendix E, *Error Codes*.

If the console response mode is enabled, the GPIB-VXI/C returns an error message in the following format:

`<error description>`<CRLF>

If both response modes are enabled, the program mode error message is returned first, followed by the console mode message.

The Help Query

The `Help?` query is a quick online reference to the syntax and functionality of the GPIB-VXI/C local command set.

Help?

Purpose

List syntax and descriptions of local command set.

Query Syntax

```
Help? [<type>[,<type>,....]]
```

or

```
Help [<type>[,<type>,....]]
```

<type> is the category of command information requested, as follows:

he	Help	ci	Code Instruments
al	All	sa	GPIB address configuration
gc	General configuration	ih	Interrupt handler configuration
dc	Dynamic configuration	ba	VXIbus access
rc	Dynamic reconfiguration	ws	Word Serial communication
rm	Resource Manager	tr	TTL trigger access
cc	Common commands		

The default type lists the categories available.

Response

The local command set is displayed in the following format:

```
      GPIB-VXI Local Command Set<CRLF>
   Command/Query Format       Description<CRLF>

<Command Syntax>            <Command description><CRLF>
<Command Syntax>            <Command description><CRLF>
<Command Syntax>            <Command description><CRLF>
      •                           •
      •                           •
      •                           •
```

Example

List syntax and descriptions of general configuration and GPIB address commands.

```
Help? gc,sa
```

General Configuration Commands and Queries

These general configuration commands and queries are described in the following sections:

- CONF
- ConsoleEna
- ConsMode
- DIAG
- DPRAM?
- NVconf?
- OBRAM?
- ProgMode
- WordSerEna

The ConsMode and ProgMode commands enable and disable the console and program response modes for the port originating the command.

The ConsoleEna and WordSerEna commands control access to the local command set from the RS-232 and VXI Word Serial ports.

The NVconf? query returns the contents of the onboard nonvolatile memory. CONF reboots the GPIB-VXI/C and enters the nonvolatile configuration editor.

DIAG reboots the GPIB-VXI/C and enters diagnostic mode.

The OBRAM? query can be used to determine the amount of GPIB-VXI/C installed RAM, and the DPRAM? query returns the amount of the installed RAM that is shared with VXI A24 space.

CONF

Purpose

Reboot into nonvolatile configuration mode.

Command Syntax

```
CONF
```

Example

Reboot into nonvolatile configuration mode.

```
CONF
```

ConsoleEna

Purpose

Enable or disable the RS-232 port as the console.

Command Syntax

```
ConsoleEna <Boolean>
```

Action

If `<Boolean>` is TRUE, `ConsoleEna` sets the RS-232 port to be a local command set input.

If `<Boolean>` is FALSE, `ConsoleEna` disables the RS-232 port connection to the local command set. Notice that once the console has been disabled, it must be re-enabled from a command source other than the RS-232 port (such as the GPIB port).

Examples

Disable console.

```
ConsoleEna 0
```

Enable console.

```
ConsoleEna 1
```

ConsMode

Purpose

Enable or disable the console data mode.

Command Syntax

`ConsMode <Boolean>`

Action

If `<Boolean>` is TRUE, `ConsMode` enables console format responses for the command source issuing the command.

If `<Boolean>` is FALSE, `ConsMode` disables console format responses for the command source issuing the command.

The console response mode applies only to the response path connected to the `ConsMode` command source. For example, disabling the console response mode from the GPIB port does not affect the response mode on the serial port.

Example

Disable console format responses.

```
ConsMode 0
```

Enable console format responses.

```
ConsMode 1
```

DIAG

Purpose

Reboot into diagnostics mode.

Command Syntax

`DIAG`

Example

Reboot into diagnostics mode.

```
DIAG
```

DPram?

Purpose

Get the A24/A32 starting address and the size of the GPIB-VXI/C VXI shared RAM.

Query Syntax

```
DPram?
```

Response

Program response:

`<A24/A32 starting address>, <shared RAM size>`<CRLF>

Console response:

```
This GPIB-VXI has <shared RAM size>K bytes dual ported to [A24, A32]
Address <A24/A32 hex starting address>
```
<CRLF>

where `<A24/A32 starting address>` is the shared RAM base address in decimal integer format,

`<shared RAM size>` is in KB.

`<A24/A32 hex starting address>` is in C language hexadecimal format.

NVconf?

Purpose

Display the contents of the nonvolatile (NV) configuration parameter memory.

Query Syntax

```
NVconf?
```

Response

The contents of the onboard EEPROM are displayed in the following format:

```
=============== Nonvolatile Configuration Information ===============

 Logical Address: 0x 0             Device Type    : Message Based
 Manufacturer Id: 0xff6            Model Code     : 0x ff (Slot 0)
 Slave Addr Spc : A24              Protocol Reg   : 0x ff0
 RESET Config   : PBtoLocalRESET PBtoSYSRESET SYSRESETtoLocalRESET

 Serial Number  : 0x   10003       User pROBE Pars: 0x     0 (None)
 Region 1 Size  : 0x070000         Number Procs   : 32
 Number Exchgs  : 32               Number Msgs    : 384
 Console        : Enabled
 VXI Interrupt Level To Handler Logical Address (0xff = free to
assign):
   1:0xff,  2:0xff,  3:0xff,  4:0xff,  5:0xff,  6:0xff,  7:0xff
 A24 Assign Base: 0x200000         A32 Assign Base: 0x20000000
 DC Starting LA : 0x 1,  BNO=YES   For FAILED Dev : DO set Reset Bit
 Servant Area   : 0x 0             GPIB Primary   : 0x 1
 GPIB Addr Assgn: Default          GPIB Flags     : NAT4882 DMA

CI Block Base  : 0x 80000         CI Num Blocks  : 0

             ------ Resident Code Instrument Locations ------
# 0:         0            # 1:         0            # 2:         0
# 3:         0            # 4:         0            # 5:         0
# 6:         0            # 7:         0            # 8:         0
# 9:         0            # a:         0            # b:         0
```

```
          ------ CI Nonvolatile User Configuration Variables ------
# 0:      0         # 1:      0         # 2:      0         # 3:      0
# 4:      0         # 5:      0         # 6:      0         # 7:      0
# 8:      0         # 9:      0         #10:      0         #11:      0
#12:      0         #13:      0         #14:      0         #15:      0
#16:      0         #17:      0         #18:      0         #19:      0
#20:      0         #21:      0         #22:      0         #23:      0
#24:      0         #25:      0         #26:      0         #27:      0
#28:      0         #29:      0         #30:      0         #31:      0
```

OBram?

Purpose

Get the amount of RAM installed onboard the GPIB-VXI/C.

Query Syntax

`OBram?`

Response

Program response:

`<memsize>`<CRLF>

where `<memsize>` is the amount of installed RAM, in KB.

Console response:

`This GPIB-VXI has <expression> of RAM installed onboard.`<CRLF>

where `<expression>` is the amount of installed RAM.

ProgMode

Purpose

Enable or disable the program data mode.

Command Syntax

`ProgMode <Boolean>`

Action

If `<Boolean>` is TRUE, `ProgMode` enables program format responses for the command source issuing the command.

If `<Boolean>` is FALSE, `ProgMode` disables program format responses for the command source issuing the command.

The program response mode applies only to the response path connected to the `ProgMode` command source. For example, disabling the program response mode from the GPIB port does not affect the response mode on the serial port.

Examples

Disable program format responses.

```
ProgMode 0
```

Enable program format responses.

```
ProgMode 1
```

WordSerEna

Purpose

Assign control of the GPIB-VXI/C physical Word Serial registers to an onboard logical address (GPIB-VXI/C command interpreter or code instrument).

Command Syntax

```
WordSerEna <logical address>
```

Action

Control of the physical Word Serial registers is passed to `<logical address>`. `<logical address>` must be the logical address of the GPIB-VXI/C or an onboard code instrument.

The default control of the physical registers is given to the GPIB-VXI/C local command set parser.

Examples

Pass control of the physical registers to code instrument at Logical Address 5.

```
WordSerEna 5
```

Pass control of the physical registers back to GPIB-VXI/C local command parser at Logical Address 0.

```
WordSerEna 0
```

RM Information Queries

These RM information queries are described in the following sections:

- A24MemMap?
- A32MemMap?
- Cmdr?
- CmdrTable?
- Laddrs?
- NumLaddrs?
- RmEntry?
- Srvnts?
- StatusState?

Note The system information commands (NumLaddrs?, Laddrs?, CmdrTable?, A24MemMap?, and A32MemMap?) return information about the known system. If the GPIB-VXI/C is the system RM, it can access information about the entire system. If it is not the RM, it has information only about itself and its immediate Servants.

The Numladdrs? query is used to find out how many devices there are in the system. The number of devices could then be used by a control program to determine the allocation size for an array that is to hold the logical addresses of each device.

The Laddrs? query returns a list of logical addresses for devices in the system.

The RmEntry?, Srvnts?, Cmdr?, and StatusState? queries return RM information for a particular device.

The CmdrTable? query returns the system hierarchy table.

The A24MemMap? and A32MemMap? queries return the A24 and A32 memory configuration lists.

A24MemMap?

Purpose

Get the A24 address space allocation for the system.

Query Syntax

```
A24MemMap?
```

Response

Program response:

```
<la1>,<A24 memory base>,<A24 memory size><CRLF>
<la2>,<A24 memory base>,<A24 memory size><CRLF>
    •
    •
<laN>,<A24 memory base>,<A24 memory size><CRLF>
```

where <la1> through <la*N*> are logical addresses containing A24 address space.

Console response:

```
A24 Memory Map is as follows:<CRLF>
Logical Address <la1> has <A24 memory size>K
<A24 memory size> bytes) at A24 Address<A24 memory base><CRLF>
    •
    •
Logical Address <laN> has <A24 memory size>K
(<A24 memory size> bytes) at A24 Address<A24 memory base><CRLF>
```

Example

Get A24 address map for the system.

```
A24MemMap?
```

A32MemMap?

Purpose

Get the A32 address space allocation for the system.

Query Syntax

```
A32MemMap?
```

Response

Program response:

```
<la1>,<A32 memory base>,<A32 memory size><CRLF>
<la2>,<A32 memory base>,<A32 memory size><CRLF>
    •
    •
<laN>,<A32 memory base>,<A32 memory size><CRLF>
```

where <la1> through <la*N*> are logical addresses containing A32 address space.

Console response:

```
A32 Memory Map is as follows:<CRLF>
Logical Address <la1> has <A32 memory size>K
(<A32 memory size> bytes) at A32 Address<A32 memory base><CRLF>
    •
    •
Logical Address <laN> has <A32 memory size>K
(<A32 memory size> bytes) at A32 Address<A32 memory base><CRLF>
```

Example

Get A32 address map for the system.

```
A32MemMap?
```

Cmdr?

Purpose

Get the logical address of a device's Commander.

Query Syntax

```
Cmdr? <logical address>
```

where `<logical address>` is the logical address of the device.

Response

Program response:

```
<Commander's logical address><CRLF>
```

Console response:

```
The Commander of Logical Address <logical address> is Logical Address
<Commander's logical address><CRLF>
```

Example

Get the Commander's logical address for Logical Address 15.

```
Cmdr? 15
```

CmdrTable?

Purpose

Get the known system hierarchy table.

Query Syntax

```
CmdrTable?
```

Response

Program response:

<cla0>,<cla1>,<cla2>,<cla3>,<cla4>, . . .,<cla254><CRLF>

where <cla*N*> is either the Commander's logical address for Logical Address *N*, or 0 for top-level Commanders and unused logical addresses. Notice that no value is returned for Logical Address 255.

Console response:

Known Hierarchy is as follows:<CRLF>
Logical address <la1> has Servants: <sa1,1>,...,<sa1,M>
<comment><CRLF>
Logical address <la2> has Servants: <sa2,1>,...,<sa2,M>
<comment><CRLF>

-
-

Logical address <la*N*> has Servants: <sa*N*,1>,...,<sa*N*,M>
<comment><CRLF>

where <la X> is a valid logical address with Servant addresses <sa *X*,1> through <sa1,M>.

The <comment> field indicates any relevant information about the status and/or capabilities of the device at Logical Address <la*X*>.

Laddrs?

Purpose

Get a list of the known logical addresses.

Query Syntax

`Laddrs?`

Response

Program response:

`<la1>,<la2>,..., <laN>`<CRLF>

where `<la1>` through `<laN>` are the known logical addresses.

Console response:

`Known logical addresses are: <la1>,<la2>,..., <laN>`<CRLF>

CI logical addresses are terminated with an asterisk (*) in the console mode response.

NumLaddrs?

Purpose

Get the number of known logical addresses.

Query Syntax

`NumLaddrs?`

Response

Program response:

`<num las>`<CRLF>

where `<num las>` is the number of known logical addresses.

Console response:

`There are <num las> known Logical Addresses`<CRLF>

RmEntry?

Purpose

Return RM information about a device or all devices. `RmEntry?` does not return the Servant list.

Query Syntax

```
RmEntry? [<logical address>]
```

If `<logical address>` is omitted, `RmEntry?` returns the RM information for all devices.

Response

Program response:

```
<la>,<cla>,<sa>,<slot>,<devclass>,<subclass>,<manID>,<modelcode>,
<memspace>,<membase>,<memsize>,<state>,<line status><CRLF>
```

Console response:

```
Resource manager entry for Logical Address <logical address>:<CRLF>
<CRLF>
Commander's Logical Address   :<cla><CRLF>
GPIB Secondary Address        :<addr><CRLF>
Slot                          :<slot><CRLF>
Device class                  :<devclass> (class)<CRLF>
Extended Sub Class            :<subclass><CRLF>
Manufacturer's ID             :<manID> (manufacturer's name)<CRLF>
Model code                    :<modelcode><CRLF>
A16/A24/A32 Memory space      :<memspace> (memory space)<CRLF>
A24/A32 Memory Base           :<membase><CRLF>
A24/A32 Memory Size           :<memsize>K (<memsize> bytes)<CRLF>
Status State                  :<state> (state)<CRLF>
Forced Offline?               :<line status> (yes/no)<CRLF>
```

The mnemonics have the following meanings:

`la`	Device's logical address
`cla`	Commander's logical address
`addr`	Device's GPIB address (255 if not assigned GPIB address)
`slot`	Slot number (255 if unknown, such as if the device does not have MODID capability)

devclass	Device class; the following values may be used: 0 = Memory Class 1 = Extended Class 2 = Message-Based 3 = Register-Based
subclass	Extended class device's subclass
manID	Manufacturer's ID number
modelcode	Device's manufacturer-assigned model code
memspace	Memory space requirement: 0 = A16 only 1 = A16/A24 2 = A16/A32
membase	Memory base address
memsize	Memory size in bytes
state	Status state: 0 = Failed and not Ready 1 = Passed and not Ready 2 = Failed and Ready 3 = Passed and Ready
line status	Online/offline status: 0 = online 1 = forced offline

The program mode response format is the same for all devices. However, the console mode response returns only the lines that are relevant. For example, memory base address and memory size lines are not returned for A16-only memory space devices.

Example

Get RM information for a device at Logical Address 78.

```
RmEntry? 78
```

Srvnts?

Purpose

Get a list of a device's Servants.

Query Syntax

```
Srvnts? <logical address>
```

`<logical address>` is the device's logical address.

Response

Program response:

`<sla1>,<sla2>,...,<slaN>`<CRLF>

where `<sla1>` through `<slaN>` are the Servant device logical addresses.

Console response:

```
Logical Address <logical address> has servants:
<sla1>, <sla2>,..., <slaN> <comment>
```
<CRLF>

if the device has Servants, or

```
Logical Address <logical address> has servants:
none <comment>
```
<CRLF>

if the device has no Servants.

The `<comment>` field indicates any relevant information about the status and/or capabilities of the device.

Example

Get a list of Servants for device at Logical Address 15.

```
Srvnts? 15
```

StatusState?

Purpose

Get a device's current self-test status.

Query Syntax

```
StatusState? <logical address>
```

`<logical address>` is the logical address for the device.

Response

Program response:

`<val>`<CRLF>

The value of `<val>` is equivalent to the value of the field in the device's status register containing the Ready and Passed bits. `<val>` can be interpreted as follows:

`0` The device is Failed and not Ready.
`1` The device is Passed and not Ready.
`2` The device is Failed and Ready.
`3` The device is Passed and Ready.

Console response:

`Device at Logical Address <logical address> is Failed and not Ready`<CRLF>

or

`Device at Logical Address <logical address> is Passed and not Ready`<CRLF>

or

`Device at Logical Address <logical address> is Failed and Ready`<CRLF>

or

`Device at Logical Address <logical address> is Passed and Ready`<CRLF>

Example

Get self-test status for device at Logical Address 48.

```
StatusState? 48
```

Dynamic Configuration Commands and Queries

These dynamic configuration (DC) commands and queries are described in the following sections:

- `DCBNOSend`
- `DCGrantDev`
- `DCSystem?`

The DC commands are used to configure the VXI system when all of these conditions are present:

- The GPIB-VXI/C is the RM.
- At least one DC device is present in the system.
- The nonvolatile configuration setup specifies *not* to send *Begin Normal Operation* (user-specified hierarchy).
- The system is still in the startup Configure substate (`DCBNOSend` has not been sent).

The `DCSystem?` query response indicates whether the system contains a DC device. If the system is found to be a DC system, the `DCGrantDev` command is used to configure the Commander/Servant hierarchy. The `DCBNOSend` command is used to end the DC phase and to cause the system to enter normal operation.

DCBNOSend

Purpose

Cause a DC system to exit the Configure substate and enter the Normal Operation substate.

Command Syntax

```
DCBNOSend
```

Action

Send the *Begin Normal Operation* command to all top-level Commanders.

DCGrantDev

Purpose

Grant a device to a Message-Based Commander in a DC system. `DCGrantDev` can be used only to configure the initial Commander/Servant hierarchy of a DC system, and before `DCBNOSend` is used to cause the system to enter the Normal Operation substate.

Command Syntax

```
DCGrantDev <Commander's logical address>,
<Servant's logical address>
```

Action

`DCGrantDev` sends the *Device Grant* command to the Commander at `<Commander's logical address>`, granting it the device at `<Servant's logical address>`.

Example

Grant Servant at Logical Address 7 to Commander at Logical Address 5.

```
DCGrantDev 5,7
```

DCSystem?

Purpose

Determine if the system is a DC system. A system is DC if it has at least one DC device.

Query Syntax

```
DCSystem?
```

Response

Program response:

`1` <CRLF>

if it is a DC system, or

`0` <CRLF>

if it is not a DC system, or if it is no longer dynamically configurable because the *Begin Normal Operation* command has already been sent to the top-level Commanders through the `DCBNOSend` local command.

Console response:

`This IS a Dynamic Configured system.`<CRLF>

if it is a DC system, or

`This is NOT a Dynamic Configured system.`<CRLF>

if it is not a DC system.

Dynamic Reconfiguration Queries

These dynamic reconfiguration queries are described in the following sections:

- `Broadcast?`
- `GrantDev?`
- `RelSrvnt?`

The dynamic reconfiguration commands are used to reconfigure the GPIB-VXI/C's Servant subtree after the system has entered the Normal Operation substate. If the GPIB-VXI/C is RM, these commands can be used to reconfigure the entire system.

The `Broadcast?` query can be used to make the system or subtree enter the Configure substate by broadcasting the *End Normal Operation* Word Serial query, or the *Clear* Word Serial command followed by the *Abort Normal Operation* Word Serial query.

The `RelSrvnt?` and `GrantDev?` queries can then be used to restructure the Commander/Servant hierarchy. You could perform dynamic reconfiguration directly by using the `WSCmd` and `WSCmd?` local commands, but the GPIB-VXI/C's RM table would not be updated. By using the `RelSrvnt?` and `GrantDev?` queries to reconfigure the system, you ensure that the GPIB-VXI/C's system hierarchy and GPIB address link records do not become corrupted.

You can return the system or subtree to the Normal Operation substate by using the `Broadcast?` query to broadcast the *Identify Commander* and *Begin Normal Operation* Word Serial commands.

Broadcast?

Purpose

Broadcast dynamic reconfiguration, initialization, or termination Word Serial commands to the GPIB-VXI/C's Message-Based Servants or to all top-level Commanders in the system.

Query Syntax

```
Broadcast? <Boolean>,<ws cmd>
```

If <Boolean> is 1, the GPIB-VXI/C broadcasts <ws cmd> to all top-level Commanders. If <Boolean> is 0, it broadcasts <ws cmd> to its Message-Based Servants. Notice that the GPIB-VXI/C should only broadcast to top-level Commanders when it is RM.

The Broadcast? query can fail due to inability to complete a Word Serial operation, or because an invalid code was returned from a device in response to ANO or ENO.

<ws cmd> is a mnemonic as follows.

<ws cmd>	Word Serial Command Name	Type
ANO	*Abort Normal Operation*	Query
BNO	*Begin Normal Operation*	Query
CLR	*Clear*	Command
ENO	*End Normal Operation*	Query
IDN	*Identify Commander*	Command

Response

Program response:

<CRLF>

if the command was successful, or

```
<la>,<cmd val>,<ws response>,<ws error code>
```

if the command failed.

Console response:

```
Done broadcasting Word Serial command: <Word Serial command name>.
```

if the command was successful, or

```
Logical address <la> returned <ws response> from ENO (Unable to halt)
```

or

```
Logical address <la> returned <ws response> from ANO (Invalid
response)
```

or

```
Error sending Logical Address <la> Word Serial command <hex cmd
val><CRLF><space><space><ws error><CRLF>
```

if the command failed.

<la> is the logical address of the device to which the broadcast failed.

<cmd val> is the value of the Word Serial command, in decimal. <hex cmd val> is the value in hexadecimal.

For Word Serial queries, <ws response> is the Word Serial response of the device at Logical Address <la>. For Word Serial commands <ws response> is 0.

<Word Serial command name> is the name of the command name as shown in the previous table.

<ws error code> is a decimal value that can be interpreted by converting it to a binary bit pattern. A value of 1 in the bit positions shown in the following table indicates that an error occurred during the attempt to broadcast the Word Serial command.

Bit	Word Serial Error
0	Word Serial command completed successfully (no Word Serial error)
1	Timeout waiting to send Word Serial command to device at <la>
2	Timeout waiting for Word Serial response from device at <la>
3	Device at <la> did not recognize the command
6	Multiple query error
10	Read Protocol error not supported
13	Read Ready (RR) violation
14	Write Ready (WR) violation

None of the other bits has significance in this context.

<ws error> is a string explaining the Word Serial error as shown in the previous table.

Example

Broadcast the *Identify Commander* Word Serial command to all top-level Commanders.

```
broadcast? 1,IDN
```

GrantDev?

Purpose

Grant a Servant to a Commander.

Query Syntax

```
GrantDev? <Commander's logical address>, <Servant's logical address>
```

Action

Grants the device at `<Servant's logical address>` to device at `<Commander's logical address>`.

The GPIB-VXI/C must own the device at `<Servant's logical address>`.
The GPIB-VXI/C can get ownership of any device with the `RelSrvnt?` command.

Notice that before the `GrantDev?` query is used, the Word Serial *End Normal Operation* query, or a *Clear* command followed by the *Abort Normal Operation* query should have been broadcast with the `Broadcast?` query.

Response

Program response:

`0`<CRLF>

indicates that the command was successful.

Console response:

```
Logical Address <Commander's logical address> granted device at
Logical Address <Servant's logical address>.
```

Example

Grant Device 16 to Commander at Logical Address 8.

```
Grantdev? 8,16
```

RelSrvnt?

Purpose

Recover a Servant from a Commander.

Query Syntax

```
RelSrvnt? <Commander's logical address>, <Servant's logical address>
```

Action

Commands device at `<Commander's logical address>` to release ownership of the device at `<Servant's logical address>`. The GPIB-VXI/C assumes ownership of the device.

Response

Program response:

`65534`<CRLF>

if the Commander released the Servant. Any other response indicates that an error occurred.

Console response:

```
Logical Address <Commander's logical address> released device at
Logical Address <Servant's logical address>.
```

Example

Recover Servant at Logical Address 16 from Commander at Logical Address 8.

```
Relsrvnt? 8,16
```

VXI-Defined Common ASCII System Commands

These VXI-defined Common ASCII System Commands and Queries are described in the following sections:

- DCON?
- DINF?
- DLAD?
- DNUM?
- DRES?
- RREG?
- WREG

You can use these commands and queries to retrieve device information/configuration, perform a soft reset, and peek/poke a device's registers.

The DNUM? query is used to find out how many devices are in the system. The DLAD? query returns a list of logical addresses for devices in the system.

The DINF? query returns static information about a device. The DCON? query returns configuration information about a device.

The DRES? query is used to perform a soft-reset sequence on a device.

The RREG? query and WREG command are used to peek (read from) and poke (write to) registers on a VXI device.

DCON?

Purpose

Return system configuration information about a device or all devices.

Query Syntax

```
DCON? [<logical address>]
```

If <logical address> is omitted, DCON? returns the configuration information for all devices.

Response

Program response:

```
<la1>,<cla>,<IHANS>,<INTS>,<status>,<sstate>,<com><CRLF>
```

Console response:

```
Device configuration at Logical Address <la>: <CRLF>
<CRLF>
Commander's Logical Address   :<cla><CRLF>
Interrupt Handlers            :<IHANS><CRLF>
Interrupters                  :<INTS><CRLF>
Passed/Failed/Ready           :<status><CRLF>
Device Substate               :<sstate><CRLF>
Manufacturer Specific Comment :<com><CRLF>
```

The mnemonics have the following meanings:

la	Device's logical address
cla	Commander's logical address
IHANS	Interrupt handler levels used by this device where IHANS is a 7-digit binary representing the seven VXI interrupt levels and a 1 in each position, meaning Interrupt Handler present
INTS	Interrupter levels used by this device where INTS is a 7-digit binary representing the seven VXI interrupt levels and a 1 in each position, meaning Interrupter present
status	Status state of the device: PASS FAIL IFAIL READY

`sstate`	Substate of the device
	NOP
	CONF
	NONE
`com`	Not used; always returns `""`

Example

Get device configuration information for Logical Address 6.

```
DCON? 6
```

DINF?

Purpose

Return static system information about a device.

Query Syntax

```
DINF? [<logical address>]
```

If <logical address> is omitted, DINF? returns static information for all devices.

Response

Program response:<CRLF>

```
<la1>,<manID>,<modelcode>,<devclass>,<memspace>,<membase>,
<memsize>,<slot>,<slot0>,<ext>,<attr>,<com><CRLF>
```

Console response:

```
Device configuration at Logical Address <la>:<CRLF>
<CRLF>
Manufacturer ID Number        :<manid> (manufacturer name)<CRLF>
Model Code                    :<modelcode><CRLF>
Device Class                  :<devclass><CRLF>
A16/A24/A32 Memory Space      :<memspace><CRLF>
A16/A24/A32 Memory Base       :<membase><CRLF>
A16/A24/A32 Memory Size       :<memsize><CRLF>
Slot                          :<slot><CRLF>
Slot 0 Logical Address        :<slot0><CRLF>
Extended Subclass             :<ext><CRLF>
Attribute                     :<attr><CRLF>
Manufacturer Specific Comment :<com><CRLF>
```

The mnemonics have the following meanings:

la	Device's logical address
manid	Manufacturer's ID number
devclass	Device class; the following values may be used: REG = Register-Based device MSG = Message-Based device EXT = Extended-Class device MEM = Memory-Based device
memspace	Memory space requirement A16 A16/A24 A16/A32

membase	Memory-based address for A16, A24, A32 "HHHH, HHHHHH, HHHHHHHH"
	memsize Memory sizes for A16, A24, A32 "HHHH, HHHHHH, HHHHHHHH"
slot	Slot number (–1 if unknown)
slot0	Slot 0 Logical Address (–1 if unknown)
ext	Extended device's subclass
attr	Memory device's attributes
com	Not used, always ""

DLAD?

Purpose

Get a list of the known logical addresses.

Query Syntax

```
DLAD?
```

Response

Program response:

<la1>,<la2>,..., <la*N*><CRLF>

where <la1> through <la*N*> are the known logical addresses.

Console response:

Known logical addresses are <la1>,<la2>,..., <la*N*><CRLF>

CI logical addresses are terminated with an asterisk (*) in the console mode response.

Example

Get a list of the known logical addresses.

```
DLAD?
```

DNUM?

Purpose

Get the number of the known logical addresses.

Query Syntax

```
DNUM?
```

Response

Program response:

<num las><CRLF>

where <num las> is the number of known logical addresses.

Console response:

There are <num las> known Logical Addresses.<CRLF>

Example

Get the number of the known logical addresses.

```
DNUM?
```

DRES?

Purpose

Perform a soft-reset sequence on a device.

Query Syntax

```
DRES? <logical address> [, <sysfail flag>]
```

Note If the device stays failed for five seconds after the soft-reset sequence, `<sysfail flag>` determines whether or not the device is kept sysfail-inhibited.

Response

Program response:

`<status>`<CRLF>

Console response:

`Logical Address <logical address> is <status>. SYSFAIL Inhibit is <state>.`<CRLF>

where `<status>` is one of the following:

PASS

FAIL

IFAIL

READY

and `<state>` is one of the following:

ON

OFF

Example

Soft-reset device at Logical Address 3.

```
DRES? 3
```

RREG?

Purpose

Read a 16-bit VXI register from a device.

Query Syntax

```
RREG? <logical address>, <reg offset>
```

where <logical address> is the device to read from and <reg offset> is the number of bytes to offset from the base of the VXI registers for that device.

Response

Program response:

<hex word value><CRLF>

Console response:

```
Value 0x<hex word value> (<word value>) read from Logical Address
<logical address>, Register offset 0x<reg offset><CRLF>
```

Example

Read Device Type register from Logical Address 12.

```
RREG? 12,2
```

WREG

Purpose

Write a 16-bit VXI register on a particular device.

Query Syntax

```
WREG <logical address>, <reg offset>, <value>
```

where <logical address> is the device to write, <reg offset> is the register offset to write to, and <value> is the 16-bit value to write.

Action

Write <value> to <logical address>, register offset <reg offset>.

Example

Write the Data Low register for Logical Address 4 with the value 65535.

```
WREG 4,14,65535
```

GPIB Address Configuration Commands and Queries

These GPIB address configuration commands are described in the following sections:

- `LaSaddr`
- `LaSaddr?`
- `Primary?`
- `SaddrLa?`
- `Saddrs?`
- `SaDisCon`

These commands and queries configure and report the relationships between VXI logical addresses and GPIB addresses.

You can determine the GPIB-VXI/C's primary address when used for multiple GPIB secondary addressing by using the `Primary?` query from the serial port. You can determine the relationships between GPIB addresses and VXI logical addresses by using the `Saddrs?` query followed by `SaddrLa?` queries, or by using the RM information query `Laddrs?` followed by `LaSaddr?` queries.

You can assign GPIB address links to Message-Based Servants of the GPIB-VXI/C with the `LaSaddr` command. The `SaDisCon` command deletes all GPIB address links except the link to the GPIB-VXI/C local commands.

Note The letters SA or SADDR in this chapter originally stood for GPIB Secondary Address. The GPIB-VXI/C can be configured to handle multiple primary addresses as well. The terminology has been left the same to maintain backward compatibility.

LaSaddr

Purpose

Attach or detach a GPIB address to a logical address.

Command Syntax

```
LaSaddr <logical address>, <GPIB address>
```

Action

If `<GPIB address>` is not equal to 255, attach `<GPIB address>` to <logical address>.

If `<GPIB address>` is equal to 255, release `<GPIB address>` currently attached to `<logical address>`.

Attaching a GPIB address to a logical address that already has a GPIB address will cause the first GPIB address to be replaced by the new GPIB address.

Attempting to release or change a GPIB address will result in a Delete I/O Link error if any of the following conditions is true:

- The GPIB address does not exist.
- The GPIB address is addressed to talk or listen; unable to delete.
- There is still data in the GPIB address input or output queue.

Examples

Attach GPIB Address 6 to Logical Address 4.

```
LaSaddr 4,6
```

Release GPIB address currently attached to Logical Address 8.

```
LaSaddr 8,255
```

LaSaddr?

Purpose

Get the GPIB address attached to a logical address.

Query Syntax

```
LaSaddr? <logical address>
```

Response

Program response:

`<GPIB address>`<CRLF>

where `<GPIB address>` is the GPIB address attached to the logical address. A value of `255` indicates that no GPIB address is attached to the logical address.

Console response:

`Logical Address <logical address> is attached to GPIB <type> Address <GPIB address>`<CRLF>

for logical addresses with attached GPIB addresses, or

`Logical Address <logical address> is NOT attached to a GPIB <type> Address`<CRLF>

for logical addresses without attached GPIB addresses.

Example

Get the GPIB address attached to Logical Address 9.

```
LaSaddr? 9
```

Primary?

Purpose

Get a GPIB primary address.

Query Syntax

```
Primary?
```

Response

Program response:

<primary address><CRLF>

where <primary address> is the GPIB primary address of GPIB-VXI/C.

Console response:

The GPIB primary address (for Secondary Address mode) of this GPIB-VXI is <primary address><CRLF>

SaddrLa?

Purpose

Get the logical address that a GPIB address is attached to.

Query Syntax

```
SaddrLa? <GPIB address>
```

Response

Program response:

`<logical address>`<CRLF>

where `<logical address>` is the logical address that the GPIB address is attached to. A value of `255` indicates that the GPIB address is not attached to a logical address.

Console response:

`GPIB <type> Address <GPIB address> is attached to Logical Address <logical address>`<CRLF>

for a GPIB address that is attached to a logical address, or

`GPIB <type> Address <GPIB address> is NOT attached to a Logical Address`<CRLF>

for a GPIB address that is not attached to any logical address.

Example

Get the logical address attached to GPIB Address 9.

```
SaddrLa? 9
```

Saddrs?

Purpose

Get a list of GPIB addresses in use.

Query Syntax

`Saddrs?`

Response

Program response:

`<sa1>,<sa2>, . . .,<saN>`<CRLF>

where `<sa1>` through `<saN>` are the GPIB addresses currently attached to logical addresses.

Console response:

```
Current GPIB Addresses used:
<type> Address <sa1>: attached to Logical Address <la1>.
<type> Address <sa2>: attached to Logical Address <la2>.
    •
    •
<type> Address <saN>: attached to Logical Address <laN><CRLF>
```

SaDisCon

Purpose

Detach *all* GPIB address links except the GPIB address link to the GPIB-VXI/C command set.

Command Syntax

`SaDisCon`

Action

Detaches all GPIB address links from Servants of the GPIB-VXI/C.

VXIbus Interrupt Handler Configuration Commands and Queries

These interrupt handler configuration commands and queries are described in the following sections:

- `AllHandlers?`
- `AssgnHndlr`
- `HandlerLine?`
- `RdHandlers?`

The interrupt handler commands and queries configure and report the relationships between the GPIB-VXI/C interrupt handlers and VXIbus interrupt levels.

The GPIB-VXI/C has three programmable interrupter handlers. An application program can confirm this with the `RdHandlers?` query. The `AllHandlers?` and `HandlerLine?` queries return the current VXI interrupt level assignments for the handlers. The `AssgnHndlr` command can be used to change the level assignments.

AllHandlers?

Purpose

Get the VXIbus interrupt level assigned to all GPIB-VXI/C interrupt handlers.

Query Syntax

```
AllHandlers?
```

Response

Program response:

<level1>,<level2>,<level3><CRLF>

where <level1> is the interrupt level assigned to Handler 1, <level2> is the interrupt level assigned to Handler 2, and <level3> is the interrupt level assigned to Handler 3.

If <level*N*> equals 0, Interrupt Handler <handler*N*> is not assigned to an interrupt level.

Console response:

```
VXI interrupt Handler 1 assigned to interrupt level <level1><CRLF>
VXI interrupt Handler 2 assigned to interrupt level <level2><CRLF>
VXI interrupt Handler 3 assigned to interrupt level <level3><CRLF>
```

if all handlers are assigned to levels, or

```
VXI Interrupt Handler <handler> NOT assigned to any interrupt
level.<CRLF>
```

if <handler*N*> is not assigned to a level.

Example

Get the interrupt level assigned to all interrupt handlers.

```
AllHandlers?
```

AssgnHndlr

Purpose

Assign a VXIbus interrupt level to a GPIB-VXI/C interrupt handler.

Command Syntax

```
AssgnHndlr <handler>, <level>
```

where <handler> is a numeric integer quantity in the range 1 to 3, and <level> is a numeric integer quantity in the range 0 to 7.

Action

If <level> is in the range 1 to 7, VXIbus Interrupt Line <level> is assigned to Interrupt Handler <handler>.

If <level> is 0, the current VXIbus interrupt line held by Interrupt Handler <handler> is released.

Examples

Assign the Interrupt Level 6 to the GPIB-VXI/C Interrupt Handler 2.

```
AssgnHndlr 2,6
```

Release the interrupt level currently held by the GPIB-VXI/C Interrupt Handler 1.

```
AssgnHndlr 1,0
```

HandlerLine?

Purpose

Get the level assigned to a GPIB-VXI/C interrupt handler.

Query Syntax

```
HandlerLine? <handler>
```

Response

Program response:

`<level>`<CRLF>

Console response:

```
VXI interrupt Handler <handler> assigned to interrupt level
<level><CRLF>
```

`<level>` is the interrupt level assigned to handler `<handler>`. If `<level>` equals 0, Interrupt Handler `<handler>` is not assigned an interrupt level.

Example

Get the interrupt level assigned to Interrupt Handler 3.

```
HandlerLine? 3
```

RdHandlers?

Purpose

Get the number of assignable GPIB-VXI/C interrupt handlers.

Query Syntax

```
RdHandlers?
```

Response

Program response:

```
3 <CRLF>
```

Console response:

```
This GPIB-VXI has 3 configurable VXI interrupt handlers.<CRLF>
```

Example

Get the number of assignable GPIB-VXI/C interrupt handlers.

```
RdHandlers?
```

IEEE-488.2 Common Commands and Queries

These IEEE-488.2 commands and queries are described in the following sections:

- *CLS
- *ESE
- *ESE?
- *ESR?
- *IDN?
- *OPC
- *OPC?
- *RST
- *SRE
- *SRE?
- *STB?
- *TRG
- *TST?
- *WAI

These commands conform to the minimal 488.2 requirements. Many of these 488.2 commands have limited meaning in the VXI environment, but are included for compatibility. The GPIB-VXI/C has no reason to interrupt as a 488.2 instrument. It is only a parser. All other functions of the GPIB-VXI/C are considered to be interface functions for other 488.2 VXI devices. It is the responsibility of each VXI device connected via the GPIB to the GPIB-VXI/C to implement 488.2 protocols if individual device 488.2 compatibility is required.

*CLS

488.2 Intent

Clear the device status data structures, and force them to the Operation Complete Query Idle state.

Command Syntax

```
*CLS
```

Action

None.

*ESE

488.2 Intent

Set the GPIB-VXI/C's Standard Event Status Enable (ESE) register bits.

Command Syntax

```
*ESE <byte value>
```

where `<byte value>` is the new value of the ESE register.

Action

Sets ESE to `<byte value>`.

Example

Set the ESE register to 45.

```
*ESE 45
```

*ESE?

488.2 Intent

Get the contents of the ESE register.

Query Syntax

```
*ESE?
```

Response

<ESE val><CRLF>

where <ESE val> is the current value of the ESE register. The default value is FFh.

*ESR?

488.2 Intent

Read and clear the Standard Event Status register (ESR).

Query Syntax

```
*ESR?
```

Response

<ESR val><CRLF>

<ESR val> is the current value of the ESR.

*IDN?

488.2 Intent

Get the GPIB-VXI/C's manufacturer, model, serial number, and firmware level.

Query Syntax

```
*IDN?
```

Response

"National Instruments","GPIB-VXI",<serial number>,<firmware version><CRLF>

*OPC

488.2 Intent

Cause the GPIB-VXI/C to generate the operation complete message in the ESR when all pending selected device operations have been finished.

Command Syntax

```
*OPC
```

Action

None.

Notice that because the GPIB-VXI/C only parses and routes commands, there are never any pending commands on the GPIB-VXI/C.

*OPC?

488.2 Intent

Cause the GPIB-VXI/C to place an ASCII 1 in its output queue when all pending operations have completed.

Query Syntax

```
*OPC?
```

Response

```
1 <CRLF>
```

*RST

488.2 Intent

Return a device to a known initial state.

Command Syntax

```
*RST
```

Action

None.

Other than the response mode configuration, the GPIB-VXI/C does not depart from its initial state.

*SRE

488.2 Intent

Set the device's Service Request Enable (SRE) register bits.

Command Syntax

```
*SRE <byte value>
```

where `<byte value>` is the new value of the SRE register.

Action

Sets the SRE to `<byte value>`.

Example

Set the SRE register to 120.

```
*SRE 120
```

*SRE?

488.2 Intent

Get the contents of the SRE register.

Query Syntax

`*SRE?`

Response

`<SRE val>`<CRLF>

`<SRE val>` is the current value of the SRE register. The default value is `FFh`.

*STB?

488.2 Intent

Get the contents of a device's Status Byte.

Query Syntax

`*STB?`

Response

`<STB value>`<CRLF>

where `<STB value>` is the current status of the path to the GPIB-VXI/C local command parser.

*TRG

488.2 Intent

Cause a device to execute a stored trigger sequence.

Command Syntax

`*TRG`

Action

None.

*TST?

488.2 Intent

Perform self-test and return passed or failed status.

Query Syntax

```
*TST?
```

Response

```
0 <CRLF>
```

Failure to complete the self-test is indicated by a failure to respond to this query. If the response is received, the self-test was successful.

*WAI

488.2 Intent

Prevent device from executing any further commands until the No-Operation Pending flag is TRUE.

Command Syntax

```
*WAI
```

Action

None.

VXIbus Access Commands and Queries

These VXIbus access commands and queries are described in the following sections:

- `A16`
- `A16?`
- `A24`
- `A24?`
- `SYSRESET`

The `A16` and `A24` commands can be used to poke, or write, locations in VXI A16 and A24 memory space. The `A16?` and `A24?` queries can be used to peek—or read—locations in VXI A16 and A24 memory space.

Note If your application requires block moving or higher speed accesses to or from the VXIbus address spaces, refer to Appendix A, *Using the NI-VISA Code Instrument*.

The `SYSRESET` command can be used to remotely reset the system.

A16

Purpose

Write a 16-bit value into VXI A16 space.

Command Syntax

```
A16 <A16 address>, <word value>
```

Action

Write <word value> to <A16 address>.

Example

Write A502h to VXI A16 address 4305h.

```
A16 #h4305, #hA502
```

A16?

Purpose

Read word value from VXI A16 address space.

Query Syntax

```
A16? <A16 address>
```

Response

Program response:

<word value><CRLF>

Console response:

Value <hex word value> (<word value>) read from A16 address <A16 hex address> (<A16 address>)<CRLF>

where <word value> is in decimal integer format, <hex word value> is in C language hexadecimal format, <A16 hex address> is in C language hexadecimal format, and <A16 address> is in decimal integer format.

Example

Read the ID register of Logical Address 16.

```
A16? #hc400
```

A24

Purpose

Write a 16-bit value into VXI A24 space.

Command Syntax

```
A24 <A24 address>, <word value>
```

Notice that `<A24 address>` has a valid range of 2097152 to 14680062 (`#h200000` to `#hE7FFFE`).

Action

Write `<word value>` to `<A24 address>`.

Example

Write the value A502h to VXI A24 address 504305h.

```
A24 #h504305, #hA502
```

A24?

Purpose

Read a word value from VXI A24 address space.

Query Syntax

```
A24? <A24 address>
```

Response

Program response:

`<word value>`<CRLF>

Console response:

`Value <hex word value> (<word value>) read from A24 address <A24 hex address> (<A24 address>)`<CRLF>

where `<word value>` is in decimal integer format, `<hex word value>` is in C language hexadecimal format, `<A24 hex address>` is in C language hexadecimal format, and `<A24 address>` is in decimal integer format.

Example

Read the word at A24 address 205634h.

```
A24? #h205634
```

SYSRESET

Purpose

Remotely reset system.

Command Syntax

```
SYSRESET
```

Action

Asserts the VXI backplane signal SYSRESET*.

TTL/ECL Trigger Access Commands

These TTL/ECL Trigger Access commands are described in the following sections:

- AckTrig
- DisTrigSense
- EnaTrigSense
- GetTrigHndlr
- MapTrigTrig
- SetTrigHndlr
- SrcTrig
- TrigAsstConf
- TrigCntrConf
- TrigExtConf
- TrigTickConf
- TrigToREQT
- UMapTrigTrig
- WaitForTrig

These commands can be used to directly manipulate the VXI TTL/ECL trigger lines and the front panel trigger connectors of the GPIB-VXI/C. The trigger functions are grouped into the following four categories:

- *Source trigger commands* act as a standard interface for asserting (sourcing) TTL and ECL triggers, as well as for detecting acknowledgements from accepting devices. These commands can source any of the VXI-defined trigger protocols from the GPIB-VXI/C. The source trigger commands are SrcTrig, SetTrigHndlr, and GetTrigHndlr.
- *Acceptor trigger commands* act as a standard interface for sensing (accepting) TTL and ECL triggers, as well as for sending acknowledgements back to the sourcing device. These functions can sense any of the VXI-defined trigger protocols on the GPIB-VXI/C. The acceptor trigger commands are EnaTrigSense, DisTrigSense, SetTrigHndlr, and GetTrigHndlr.

- *Map trigger commands* are configuration commands for routing and signal conditioning. You can use the `MapTrigTrig` and `UMapTrigTrig` commands to configure the GPIB-VXI/C hardware to route specified source trigger locations to destination trigger locations. You can use these commands as a cross-point switch/signal conditioning configurator.
- *Trigger configuration commands* are configuration tools for configuring not only the general settings of the trigger inputs and outputs, but also the National Instruments Trigger Interface Chip (TIC) counter and tick timers. The trigger configuration commands are `TrigAsstConf`, `TrigExtConf`, `TrigCntrConf`, `TrigTickConf`, and `TrigToREQT`. `TrigToREQT` is a special function for the GPIB-VXI/C to map trigger interrupt sources to SRQ on the GPIB so that VXI trigger protocols can be completely controlled from an external GPIB controller.

AckTrig

Purpose

Acknowledge the specified TTL/ECL or external (GPIO) trigger.

Query Syntax

```
AckTrig <line>
```

where the value of <line> corresponds to the trigger line to acknowledge.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
40 to 49	External source/destination (GPIO 0 to 9)

Response

Program response: 0

Console response:

```
Trigger acknowledged (line = <line text>).<CRLF>
```

where the meaning of <line text> corresponds to the value of <line> as follows.

Value of <line>	Value of <line text>
0 to 7	TTL <line>
8 to 9	ECL (<line> – 8)
40 to 49	GPIO (<line> – 40)

Example

Acknowledge a trigger interrupt for TTL line 4.

```
AckTrig 4
```

DisTrigSense

Purpose

Disable the sensing of the specified TTL/ECL trigger line, counter, or tick timer that was enabled by `EnaTrigSense`.

Query Syntax

```
DisTrigSense <line>
```

where the value of `<line>` corresponds to the trigger line on which to disable sensing.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
50	TIC counter
60	TIC TICK timers

Response

Program response: 0

Console response:

`Trigger sense disabling (line = <line text>) complete.`<CRLF>

where the meaning of `<line text>` corresponds to the value of `<line>` as follows.

Value of **`<line>`**	Value of **`<line text>`**
0 to 7	`TTL <line>`
8 to 9	`ECL (<line> - 8)`
50	TCNTR
60	TICK 1

Example

Disable sensing of TTL line 4.

```
DisTrigSense 4
```

EnaTrigSense

Purpose

Enable the sensing of the specified TTL/ECL trigger line or starts up the counter or tick timer for the specified protocol.

Query Syntax

```
EnaTrigSense <line>, <protocol>
```

where the value of `<line>` corresponds to the trigger line on which to enable sensing.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
50	TIC counter
60	TIC TICK timers

and the value of `<protocol>` specifies the protocol to use.

Value	Protocol
2	START
3	STOP
4	SYNC
5	SEMI-SYNC
6	ASYNC

Response

Program response: 0

Console response:

```
Trigger sense enabling (line = <line text>, protocol = <protocol
text>) complete.<CRLF>
```

where the meaning of `<line text>` corresponds to the value of `<line>` as follows.

Value of `<line>`	Value of `<line text>`
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
50	TCNTR
60	TICK 1

and the meaning of `<protocol text>` corresponds to the value of `<protocol>` as follows.

Value of `<protocol>`	Value of `<protocol text>`
2	START
3	STOP
4	SYNC
5	SEMI-SYNC
6	ASYNC

Example

Enable sensing of TTL line 4 for SEMI-SYNC protocol.

```
EnaTrigSense 4, 5
```

GetTrigHndlr

Purpose

Get the address of the current TTL/ECL trigger, counter, or tick timer interrupt handler for a specified trigger source.

Query Syntax

```
GetTrigHndlr <line>
```

where the value of `<line>` corresponds to the trigger line or counter/tick source.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
50	TIC counter
60	TIC TICK timers

Response

Program response: 0

Console response:

`Trigger handler (line = <line text>): DefaultTrigHandler().`<CRLF>

where the meaning of `<line text>` corresponds to the value of `<line>` as follows.

Value of **<line>**	Value of **<line text>**
0 to 7	`TTL <line>`
8 to 9	`ECL (<line> - 8)`
50	TCNTR
60	TICK 1

Example

Get the address of the trigger interrupt handler for TTL trigger line 4.

```
GetTrigHndlr 4
```

MapTrigTrig

Purpose

Map a specified TTL, ECL, Star X, Star Y, external connection (GPIO), or miscellaneous signal line to another.

Query Syntax

```
MapTrigTrig <srcTrig>, <destTrig>, <mode>
```

where `<srcTrig>` is the source line to map to a destination, the value of `<destTrig>` corresponds to the destination line to map from the source.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
40 to 49	External source/destination (GPIO 0 to 9)
40	Front panel In (connector 1)
41	Front panel Out (connector 2)
42	Front panel In (unbuffered)
43	Connection to EXTCLK input pin
44 to 49	Hardware-dependent GPIOs 4 to 9
50	TIC counter pulse output (TCNTR)
51	TIC counter finished output (GCNTR)
60	TIC TICK1 tick timer output
61	TIC TICK2 tick timer output

The value of <mode> specifies the signal conditioning mode (where 0 = no conditioning). The conditioning effects for bits 0 to 3 are as follows.

Bit	Conditioning Effect
0	Synchronize with next CLK edge
1	Invert signal polarity
2	Pulse stretch to one CLK minimum
3	Use EXTCLK (not CLK10) for conditioning

Response

Program response: 0

Console response:

```
Mapping complete (line = <line text source> mapped to line = <line
text destination>, mode = <mode>).<CRLF>
```

where the meaning of <line text source> and <line text destination> correspond to the value of <srcTrig> and <destTrig> as follows.

Value of <srcTrig> or <destTrig>	Value of <line text source> or <line text destination>
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
40 to 49	GPIO (<line> - 40)
50	TCNTR
51	GCNTR
60	TICK1
61	TICK2

Example

Map TTL line 4 to go out of the front panel with no signal conditioning.

```
MapTrigTrig 4, 41, 0
```

SetTrigHndlr

Purpose

Replace the current TTL/ECL trigger, counter, or tick timer interrupt handler with a specified trigger source with a specified function.

Query Syntax

```
SetTrigHndlr <lines>, <function>
```

where <lines> is a bit vector of trigger lines (1 = set; 0 = do not set), where the value corresponds to the trigger line(s) to set.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
14	TIC counter
15	TIC TICK timers

and <function> is a pointer to the new trigger interrupt handler, where the value is defined as follows.

Value	Interrupt Handler
0	Specify DefaultTrigHandler
1	Specify DefaultTrigHandler2
Other	User-installed trigger interrupt handler

Response

Program response: 0

Console response:

```
Trigger handler(s) installed (lines = <lines text>):
DefaultTrigHandler().<CRLF>
```

where the meaning of <lines text> = x, y, z..., where x, y, and z are bits that are set in <lines>.

Example

Set a trigger interrupt handler for TTL trigger line 4.

```
SetTrigHndlr 16, 0
```

Note `DefaultTrigHandler` automatically acknowledges acceptor protocols that require acknowledgement, while `DefaultTrigHandler2` does not. If `DefaultTrigHandler2` is used, send `AckTrig` to acknowledge the trigger.

SrcTrig

Purpose

Source a specified protocol on a specified TTL, ECL, or external trigger line.

Query Syntax

```
SrcTrig <line>, <protocol>, <timeout>
```

where the value of `<line>` corresponds to the trigger line to source.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
40 to 49	External source/destination (GPIO 0 to 9) (supports ON, OFF, START, STOP, and SYNC protocols only)
50	TIC counter (supports SYNC and SEMI-SYNC protocols only)
60	TIC TICK timers (supports SYNC and SEMI-SYNC protocols only)

the value of `<protocol>` specifies the protocol to use.

Value	Protocol
0	ON
1	OFF
2	START
3	STOP
4	SYNC
5	SEMI-SYNC
6	ASYNC
7	SEMI-SYNC and wait for Acknowledge

Value	Protocol
8	ASYNC and wait for Acknowledge
ffffh	Abort previous Acknowledge pending (5 and 6)

and <timeout> is the timeout value in milliseconds.

Response

Program response: 0

Console response:
Trigger sourcing (line = <line text>, protocol = <protocol text>) complete.<CRLF>

where the meaning of <line text> corresponds to the value of <line> as follows.

Value of <line>	Value of <line text>
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
40 to 49	GPIO (<line> - 40)
50	TCNTR
60	TICK 1

and the meaning of <protocol text> corresponds to the value of <protocol> as follows.

Value of <protocol>	Value of <protocol text>
0	ON
1	OFF
2	START
3	STOP
4	SYNC
5	SEMI-SYNC
6	ASYNC
7	SEMI-SYNC wait ACK

Value of <protocol>	Value of <protocol text>
8	ASYNC wait ACK
ffffh	wait ACK ABORT

Example

Source TTL line 4 for SEMI-SYNC protocol.

```
SrcTrig 4, 5, 0
```

TrigAsstConf

Purpose

Configure a specified TTL/ECL trigger line assertion method.

Query Syntax

```
TrigAsstConf <line>, <mode>
```

where the value of <line> corresponds to the trigger line to configure.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
ffffh	General assertion configuration (all lines)

and <mode> specifies the configuration mode, where

Bit	Specific Line Configuration Modes
0	1 = Synchronize falling edge of CLK10 0 = Synchronize rising edge of CLK10

Bit	General Configuration Modes
1	1 = Pass trigger through asynchronously 0 = Synchronize with next CLK10 edge
2	1 = Participate in SEMI-SYNC with external trigger acknowledge protocol 0 = Do not participate

All other values are reserved for future expansion.

Response

Program response: 0

Console response:

```
Trigger assertion configuration complete (line = <line text>,
mode = <mode>).<CRLF>
```

where the meaning of <line text> corresponds to the value of <line>.

Value of <line>	Value of <line text>
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
ffffh	GENERAL CONFIG

Example 1

Configure all TTL/ECL trigger lines generally to synchronize to the falling edge of CLK10 (as opposed to the rising edge).

```
TrigAsstConf -1, 1
```

Example 2

Configure TTL trigger line 4 to synchronize to CLK10 for any assertion method and do not participate in SEMI-SYNC.

```
TrigAsstConf 4, 0
```

TrigCntrConf

Purpose

Configure the TIC chip internal 16-bit counter.

Query Syntax

`TrigCntrConf <mode>, <source>, <count>`

where `<mode>` specifies the configuration mode.

Value	Mode
0	Initialize the counter
2	Reload the counter leaving enabled
3	Disable/abort any count in progress

`<source>` specifies the trigger line to configure as input to counter.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
70	CLK10
71	EXTCLK

and `<count>` specifies the number of input pulses to count before terminating.

Response

Program response: 0

Console response:

```
CNTR configured (mode = <mode text>, source = <source text>,
count = <count>).<CRLF>
```

where the meaning of `<mode text>` corresponds to the value of `<mode>`.

Value of `<mode>`	Value of `<mode text>`
0	INIT
2	RELOAD
3	DISABLE

and the meaning of `<source text>` corresponds to the value of `<source>`.

Value of `<source>`	Value of `<source text>`
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
70	CLK10
71	EXTCLK

Example

Configure the counter count 25 assertions on TTL trigger line 5 (the `<protocol>` parameter when calling `EnaTrigSense` will determine whether the counter accepts SYNC or SEMI-SYNC assertions).

```
TrigCntrConf 0, 5, 25
```

TrigExtConf

Purpose

Configure the external trigger (GPIO) lines.

Query Syntax

`TrigExtConf <extline>, <mode>`

where the value of `<extline>` is the trigger line to configure.

Value	Trigger Line
40 to 49	External source/destination (GPIO 0 to 9)
40	Front panel In (connector 1)
41	Front panel Out (connector 2)
42	ECL bypass from front panel
43	EXTCLK
44 to 49	Hardware-dependent GPIOs 4 to 9

and `<mode>` specifies the configuration mode, where

Bit	Configuration Modes
0	1 = Feed back any line mapped as input into the cross-point switch 0 = Drive input to external (GPIO) pin
1	1 = Assert input (regardless of feedback) 0 = Leave input unconfigured
2	1 = If assertion selected, assert low 0 = If assertion selected, assert high
3	1 = Invert external input (not feedback) 0 = Pass external input unchanged

All other values are reserved for future expansion.

Response

Program response: 0

Console response:

```
External connection (GPIO) configuration complete (extline = <extline
text>, mode = <mode>).<CRLF>
```

where the meaning of <extline text> corresponds to the value of <extline> as follows.

Value of <extline>	Value of <extline text>
40 to 49	GPIO (<extline> - 40)

Example 1

Configure external line 41 (front panel Out) to not be used as feedback and left tri-stated for use as a mapped output via MapTrigTrig.

```
TrigExtConf 41, 0
```

Example 2

Configure external line 40 (front panel In) to not be used as feedback and left tri-stated for use as a mapped input via MapTrigTrig.

```
TrigExtConf 40, 8
```

Example 3

Configure external line 48 (GPIO 8) to be used as feedback for use as a cross-point switch input and output via MapTrigTrig.

```
TrigExtConf 48, 1
```

TrigTickConf

Purpose

Configure the TIC chip internal dual 5-bit tick timers.

Query Syntax

```
TrigTickConf <mode>, <source>, <tcount1>, <tcount2>
```

where <mode> specifies the configuration mode.

Value	Mode
0	Initialize the tick timers (rollover mode)
1	Initialize the tick timers (non-rollover mode)
2	Reload the tick timers leaving enabled
3	Disable/abort any count in progress

and the value of <source> is the trigger line to configure as input to counter.

Value	Trigger Line
40 to 49	External source/destination (GPIO 0 to 9)
70	CLK10
71	EXTCLK

and the values of <tcount1> and <tcount2> are the number of input pulses (as a power of two) to count before asserting TICK1 output or TICK2 output, respectively (and terminating the tick timer if configured for non-rollover mode).

Response

Program response: 0

Console response:

```
TICKs configured (mode = <mode text>, source = <source text>,
t1 = tcount1, t2 = tcount2).<CRLF>
```

where the meaning of `<mode text>` corresponds to the value of `<mode>`.

Value of `<mode>`	Value of `<mode text>`
0	INIT w/ROLL
1	INIT w/NOROLL
2	RELOAD
3	DISABLE

and the meaning of `<source text>` corresponds to the value of `<source>`.

Value of `<source>`	Value of `<source text>`
40 to 49	`GPIO (<source> - 40)`
70	`CLK10`
71	`EXTCLK`

Example 1

Configure the tick timers to interrupt every 6.55 milliseconds by dividing down CLK10 as an input. Call `EnaTrigSense` to start the tick timers and enable interrupts.

```
TrigTickConf 0, 70, 16, 0
```

Example 2

Configure the tick timers to output a continuous 9.765-kHz square wave on TICK1 output and a 1.25-MHz clock on TICK2 output by dividing down CLK10 as an input. Call `SrcTrig` to start the tick timers.

```
TrigTickConf 0, 70, 10, 3
```

TrigToREQT

Purpose

Map trigger interrupt to GPIB SRQ condition (REQT generation for a particular GPIB address).

Command Syntax

```
TrigToREQT <la>, <line>
```

where <la> identifies the device for which to assert SRQ, and <line> is the trigger line for which to map the interrupt, where the value of <line> corresponds to the trigger line or counter/tick.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
50	TIC counter
60	TIC TICK1 tick timer

Action

The GPIB-VXI/C is set up to assert SRQ for a device attached to a GPIB address for a given trigger line's interrupt, as configured using either the SrcTrig or EnableSense function.

Response

Program response: 0

Console response:
Line: <line text>, configured to generate an REQT for Logical Address <la>.<CRLF>

where the meaning of <line text> corresponds to the value of <line> as follows.

Value of <line>	Value of <line text>
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
50	TCNTR
60	TICK1

Example

Set up Logical Address 4 to assert SRQ when a trigger interrupt occurs on TTL trigger line 2.

```
TrigToREQT 4, 2
```

UMapTrigTrig

Purpose

Unmap a specified TTL, ECL, Star X, Star Y, external connection (GPIO), or miscellaneous signal line that was mapped to another line using the `MapTrigTrig` function.

Query Syntax

```
UMapTrigTrig <srcTrig>, <destTrig>
```

where `<srcTrig>` is the source line to unmap from a destination, and the value of `<destTrig>` corresponds to the destination line mapped from the source.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
40 to 49	External source/destination (GPIO 0 to 9)
40	Front panel In (connector 1)
41	Front panel Out (connector 2)
42	Front panel In (unbuffered)
43	Connection to EXTCLK input pin
44 to 49	Hardware-dependent GPIOs 4 to 9
50	TIC counter pulse output (TCNTR)
51	TIC counter finished output (GCNTR)
60	TIC TICK1 tick timer output
61	TIC TICK2 tick timer output

Response

Program response: 0

Console response:

```
Unmapping complete (line <line text source> unmapped from line
<line text destination>).<CRLF>
```

where the meaning of <line text source> and <line text destination> correspond to the value of <srcTrig> and <destTrig>.

Value of <srcTrig> or <destTrig>	Value of <line text source> or <line text destination>
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
40 to 49	GPIO (<line> - 40)
50	TCNTR
51	GCNTR
60	TICK1
61	TICK2

Example

Unmap route of TTL line 4 to go out of the front panel as mapped by MapTrigTrig.

```
UMapTrigTrig 4, 49
```

WaitForTrig

Purpose

Wait for the specified trigger line to be sensed for the specified time. `EnaTrigSense` must be called to sensitize the hardware to the particular trigger protocol to be sensed.

Query Syntax

```
WaitForTrig <line>, <timeout>
```

where the value of `<line>` corresponds to the trigger line to wait for.

Value	Trigger Line
0 to 7	TTL trigger lines 0 to 7
8 to 9	ECL trigger lines 0 to 1
50	TIC counter
60	TIC TICK1 tick timer

Response

Program response: 0

Console response:

`Trigger received (line = <line text>), wait complete.`<CRLF>

where the meaning of `<line text>` corresponds to the value of `<line>` as follows.

Value of **<line>**	Value of **<line text>**
0 to 7	TTL <line>
8 to 9	ECL (<line> - 8)
50	TCNTR
60	TICK1

Example

Wait for TTL line 4 to be encountered.

```
WaitForTrig 4, 10000
```

Word Serial Communication Commands and Queries

These Word Serial communication commands and queries are described in the following sections:

- `ProtErr?`
- `RespReg?`
- `WScmd`
- `WScmd?`
- `WSresp?`
- `WSstr`
- `WSstr?`

You can use these commands to directly generate Word Serial communication operations with any Message-Based device, including the GPIB-VXI/C itself, regardless of whether or not it is the GPIB-VXI/C's Servant.

Note The Word Serial communication commands and queries are intended for debugging purposes. National Instruments does not guarantee that these commands will work when other Word Serial paths, such as the GPIB address link, are open.

Some of the Word Serial commands as defined in the VXIbus specification require a response from the Message-Based device, while other commands do not. To distinguish between the two types of Word Serial commands and to avoid confusion between Word Serial commands and GPIB-VXI/C local commands and queries, the following terminology will be used in this section:

- *Word Serial command*—A VXI-defined Word Serial command that does not require a response from the Message-Based device.
- *Word Serial query*—A VXI-defined Word Serial command that requires a response from the Message-Based device.
- *Command*—A GPIB-VXI/C command, as defined in this chapter.
- *Query*—A GPIB-VXI/C query, as defined in this chapter.

You can use the `WScmd` command to send a Word Serial command to a Message-Based device. The `WScmd?` query is used to send a Word Serial query to the Message-Based device, and to automatically read and return the device's response.

You can also use `WScmd` to send a Word Serial query to a Message-Based device. Because `WScmd` does not read the query response, the intermediate state of the device can be examined using the `RespReg?` query, after which the response can be read using the `WSresp?` query.

You can use the `WSstr` command to send device-dependent commands and queries to a device. If the string sent to the device was a device-dependent query, you can use the `WSstr?` query to read the device's response.

The `ProtErr?` query sends a *Read Protocol Error* Word Serial query to a device and reports the error response. The `RespReg?` query returns the value of a device's response register.

ProtErr?

Purpose

Send a *Read Protocol Error* Word Serial query to a Message-Based device.

Query Syntax

```
ProtErr? <log addr>
```

Action

Read Protocol Error query is sent to a Message-Based device. Response is read and reported.

Response

Program response:

<hex value><CRLF>

where <hex value> is the hexadecimal value of the Data Low register response.

Console response:

```
Read Protocol Error for Logical Address <log addr> returned 0x<hex
value>:
   <description>
```

where <description> is text explaining the error response.

Example

```
ProtErr? 3
```

RespReg?

Purpose

Get the Response register contents of a Message-Based device.

Query Syntax

`RespReg? <log addr>`

Action

Returns the contents of the device's Response register at Logical Address `<log addr>`.

Response

Program response:

`<hex value>`<CRLF>

where `<hex value>` is the hexadecimal value of the Response register contents.

Console response:

`Logical Address <log addr>'s Response register:`<CRLF>
`0x<hex value>]: <dor> <dir> <err> <rr> <wr> <fhs> <locked>`<CRLF>

where `<dor>`, `<dir>`, `<err>`, `<rr>`, `<wr>`, `<fhs>`, and `<locked>` are text flags that interpret the state of the Response register bit flags. Capitalized text in a text flag indicates that the corresponding bit flag is in the logic TRUE state. Lowercase text indicates that the corresponding bit flag is in the logic FALSE state.

WScmd

Purpose

Send a 16-bit Word Serial command or query to a Message-Based device.

Command Syntax

```
WScmd <log addr>, <WS cmd>
```

Action

Sends the Word Serial command `<WS cmd>` to the device at `<log addr>`.

Example

Write the *Begin Normal Operation* Word Serial query (FCFFh) to a device at Logical Address 3.

```
WScmd 3, #hFCFF
```

WScmd?

Purpose

Send a 16-bit Word Serial query to a Message-Based device.

Query Syntax

```
WScmd? <log addr>, <WS cmd>
```

Action

Sends the Word Serial query `<WS cmd>` to the device at `<log addr>`. Reads and returns the device's response.

Response

Program response:

`<hex value>`<CRLF>

where `<hex value>` is the hexadecimal value of the Data Low register response.

Console response:

`Logical Address <log addr> Word Serial Query 0xceff returned 0x<hex value>.`<CRLF>

Example

Write the *Read Servant Area* Word Serial query (CEFFh) to a device at Logical Address 4.

```
WScmd? 4, #hCEFF
```

WSresp?

Purpose

Read a 16-bit Word Serial response to a previously sent query.

Query Syntax

```
WSresp? <log addr>
```

Action

Reads and returns the response of the device at <log addr>.

Response

Program response:

<hex value><CRLF>

where <hex value> is the hexadecimal value of the Data Low register response.

Console response:

Logical Address <log addr> returned response 0x<hex value><CRLF>

Example

Read the 16-bit response to a previously sent Word Serial query from Logical Address 3.

```
WSresp? 3
```

WSstr

Purpose

Send a device-dependent command string to a Message-Based device.

Command Syntax

```
WSstr <log addr>, <string>
```

where <string> is an ASCII character sequence enclosed by double quotation marks (").

The following sequences of characters within the <string> parameter are special cases and will be interpreted as follows:

\n	linefeed (LF)
\r	carriage return (CR)
\\	backslash (\)
\xHH	any binary 8-bit value where HH is the ASCII hexadecimal representation of that value

Action

Writes the string <string> to the device at <log addr> as a series of *Byte Available* commands.

Example

Write the string "start" to a device at Logical Address 8.

```
WSstr 8, "start"
```

WSstr?

Purpose

Read a device-dependent response string from a Message-Based device.

Query Syntax

```
WSstr? <log addr>, <max cnt>
```

Action

Reads and returns a string, up to a maximum character count of `<max cnt>`, using a series of *Byte Request* commands.

Response

Program response:

```
<resp string>
```

where `<resp string>` is the response string returned by the device.

Console response:

```
Logical Address <log addr> read <# bytes> (<hex # bytes>) through Word
Serial: <CRLF><CRLF> <resp string>
```

where `<# bytes>` and `<hex # bytes>` are the number of bytes in `<resp string>`, in decimal and hexadecimal, respectively.

Example

Read a device-dependent response up to 20 characters long from a device at Logical Address 10.

```
WSstr? 10, 20
```

4

Nonvolatile Configuration

This chapter describes the method for editing and reviewing the contents of the nonvolatile memory, which is used for storing configuration information on the GPIB-VXI/C.

The GPIB-VXI/C nonvolatile (NV) memory is a 256-byte EEPROM that is accessible as 64 longword locations. The first half of the NV memory (32 longwords) is reserved for use by National Instruments. The second half of NV memory is allocated for storing Code Instrument (CI) configuration variables.

Note National Instruments no longer supports development of Code Instruments.

The configuration parameters include the following:

- Local register configuration
- pSOS configuration
- VXI interrupt line assignment
- Resource Manager (RM) A24 and A32 address assignment base
- Servant area size
- DC starting logical address and hierarchy configuration
- Device failure mode
- GPIB configuration
- Default CI configuration
- CI RAM area configuration
- Resident CI locations
- CI user configuration variables

You can enter NV configuration mode through either of the following methods:

- Set the startup mode switches to the nonvolatile configuration mode as described in the *GPIB-VXI/C Startup Mode Configuration* section of Chapter 2, *Configuration and Startup Procedures*. For this mode, set

switch S19 to the *OFF* position and set switch S20 to the *ON* position. Restart the system.

- In 488-VXI runtime system mode, you can enter NV configuration mode through the `CONF` command.

The nonvolatile configuration commands must be executed from the RS-232 port.

The EEPROM is connected to the microprocessor via an I^2C serial bus. Because it takes five to ten seconds to write the contents of the memory, the GPIB-VXI/C creates a copy of the contents of the EEPROM in RAM, which can be quickly edited. When the editing is complete, the entire contents of the RAM copy can be written back to the EEPROM.

Notice that some of the changes (such as the pSOS parameters) do not take effect until the system is restarted. This can be accomplished by the pROBE commands `IN` or `BO`, by resetting the system, or by cycling the system power.

The GPIB-VXI/C Nonvolatile Configuration Main Menu

When you enter the NV configuration mode, the GPIB-VXI/C displays the following menu.

```
      GPIB-VXI Nonvolatile Configuration Main Menu
             (C) 1995 National Instruments
================================================
1). Read In Nonvolatile Configuration
2). Print Configuration Information
3). Change Configuration Information
4). Set Configuration to Factory Settings
5). Write Back (Save) Changes
6). Quit Configuration

    Choice (1-6):
```

From the main menu, you can select the NV memory editing function you want to perform. To select an item in the menu, enter its number at the prompt. The effect of selecting each item is described below.

Read in Nonvolatile Configuration

The item `Read In Nonvolatile Configuration` reads the contents of the EEPROM into RAM.

Print Configuration Information

The item `Print Configuration Information` displays the Nonvolatile Configuration Information from the RAM copy, as shown in the following example.

```
Logical Address: 0x00             Device Type    : Message Based
Manufacturer Id: 0xFF6            Model Code     : 0x0FF (Slot 0)
Slave Addr Spc : A24              Protocol Reg   : 0x0FF0
RESET Config   : PBtoLocalRESET PBtoSYSRESET SYSRESETtoLocalRESET

Serial Number  : 0x00010003       User pROBE Pars: 0x000000 (None)
Region 1 Size  : 0x070000         Number Procs   : 0x20
Number Exchgs  : 0x20             Number Msgs    : 0x180
Console        : Enabled          RM Wait Period : 2 seconds
VXI Interrupt Level To Handler Logical Address (0xFF = free to assign):
  1:0xFF,  2:0xFF,  3:0xFF,  4:0xFF,  5:0xFF,  6:0xFF,  7:0xFF
A24 Assign Base: 0x200000         A32 Assign Base: 0x20000000
DC Starting LA : 0x01,  BNO=YES   For FAILED Dev : DO set Reset Bit
Servant Area   : 0x00             GPIB Primary   : 0x01
GPIB Addr Assgn: Default          GPIB Flags     : MultSecond NAT4882 DMA
GPIB Addr Avoid: 0x00000000

CI Block Base  : 0x080000         CI Num Blocks  : 0x00

          ------ Resident Code Instrument Locations ------
0x00: 00000000            0x01: 00000000            0x02: 00000000
0x03: 00000000            0x04: 00000000            0x05: 00000000
0x06: 00000000            0x07: 00000000            0x08: 00000000
0x09: 00000000            0x0A: 00000000            0x0B: 00000000

     ------ CI Nonvolatile User Configuration Variables ------
0x00:00000000      0x01:00000000      0x02:00000000      0x03:00000000
0x04:00000000      0x05:00000000      0x06:00000000      0x07:00000000
0x08:00000000      0x09:00000000      0x0A:00000000      0x0B:00000000
0x0C:00000000      0x0D:00000000      0x0E:00000000      0x0F:00000000
0x10:00000000      0x11:00000000      0x12:00000000      0x13:00000000
0x14:00000000      0x15:00000000      0x16:00000000      0x17:00000000
0x18:00000000      0x19:00000000      0x1A:00000000      0x1B:00000000
0x1C:00000000      0x1D:00000000      0x1E:00000000      0x1F:00000000
```

The first four sections display the National Instruments-reserved variables. The last section displays hexadecimal values representing the contents of the user-defined variables. In this example, no user-defined variables have been initialized.

The following sections describe the fields in the Nonvolatile Configuration Information Display.

Logical Address

This field contains the VXI logical address of the GPIB-VXI/C. It specifies the location of the GPIB-VXI/C registers in VXI A16 space. The formula is as follows:

```
C000h + (40h * Logical Address)
```

If the Logical Address is set to 0, the GPIB-VXI/C will attempt to be the VXI Resource Manager. If the Logical Address is set in the range of 01 to FEh (1 through 254), the GPIB-VXI/C is set up to be a Static Configuration (SC) Message-Based (or possibly Register-Based) device. If the Logical Address is set to FFh (255), the GPIB-VXI/C is set up to be a Dynamic Configuration (DC) Message-Based (or possibly Register-Based) device. The factory setting is Logical Address 0.

Device Type

You can set up the GPIB-VXI/C to be either a Message-Based or a Register-Based VXI device. Normally, the GPIB-VXI/C should be a Message-Based device. In Register-Based mode, however, the GPIB-VXI/C can reside virtually transparently in the VXI system for use as a debugging tool. It can still access the VXIbus directly as a bus master, perform Word Serial operations and GPIB transactions, and use Code Instruments. None of the functionality is removed; however, the Resource Manager does not grant any Servants to a Register-Based GPIB-VXI/C.

Manufacturer Id

The Manufacturer Id is set at the factory and cannot be changed. Manufacturer Ids are assigned by the VXI Consortium. The Manufacturer Id for National Instruments is FF6h.

Model Code, Slot 0/Non-Slot 0

You can configure the GPIB-VXI/C for either Slot 0 or Non-Slot 0 operation. According to the VXIbus specification, a device configured to be in Slot 0 must have a Model Code between 000h and 0FFh. A device

configured to be in a slot other than Slot 0 must have a Model Code greater than 0FFh. The GPIB-VXI/C Model Codes are assigned by National Instruments. This field is used only to configure which one of the two GPIB-VXI/C Model Codes to use. The factory setting is for Slot 0.

Slave Address Space

The GPIB-VXI/C can be configured to share 0%, 25%, 50%, or 100% of its onboard RAM with the VXIbus in either A24 or A32 address spaces. The percentage shared with the VXIbus is set via switches S1 and S2. Refer to Table 2-4, *Shared Memory Switch Settings*, for more information. The VXI address space to be shared with the local RAM is set with this field in nonvolatile configuration mode. The factory setting is 0% dual-ported RAM.

Protocol Register

You can configure the GPIB-VXI/C to have a user-defined Protocol register. Only the FHS* and INT bits are not permitted to be active.

RESET Configuration

The GPIB-VXI/C has three configurable reset parameters. They can be enabled or disabled and are as follows:

- Pushbutton resets backplane (asserts SYSRESET* signal).
- Pushbutton resets GPIB-VXI/C (asserts local reset signal).
- Backplane SYSRESET* signal resets GPIB-VXI/C (SYSRESET* on backplane asserts local reset).

Serial Number

The serial number is a 32-bit quantity used to identify a particular GPIB-VXI/C. This value is set at the factory and cannot be altered.

pSOS Region 1 Size

pSOS Region 1 is the Dynamic Memory pool used for the majority of memory requirements of the GPIB-VXI/C. All process control blocks (PCBs), process stacks, queues, messages, GPIB buffers, and so on, are allocated from this region. The first 64 KB (0 to FFFFh) of any size onboard RAM configuration are reserved for use by National Instruments. You can allocate the rest for Region 1, Code Instruments, or a

device-dependent use. Region 1 always starts at local address 10000h. The minimum size is 60000h. The maximum size is the amount of RAM minus 10000h.

Number of pSOS Processes

You can use this parameter to configure the maximum allowable number of pSOS processes. The GPIB-VXI/C requires a minimum of 16 processes. The factory setting is 32.

Number of pSOS Message Exchanges

You can use this parameter to configure the maximum allowable number of pSOS message exchanges. The GPIB-VXI/C requires a minimum of 16 message exchanges. The factory setting is 32.

Number of pSOS Message Buffers

You can use this parameter to configure the maximum allowable number of pSOS message buffers. The GPIB-VXI/C requires a minimum of 100h message buffers. The factory setting is 180h.

Console

You can use this parameter to set the GPIB-VXI/C RS-232 local command console to default to enabled or disabled. You can use the local command `ConsoleEna` to change the setting at runtime.

Resource Manager Wait Period

You can use this parameter to specify how many seconds the Resource Manager waits for devices to boot before starting setup of the VXI system.

VXI Interrupt Level to Handler Logical Address

This is a table of logical addresses the Resource Manager can use during resource management of the VXI interrupt lines. If an interrupter is hard-configured (not a VXI programmable interrupter), place the logical address of the interrupt handler device in the corresponding level. If an interrupt handler is hard-configured (not a VXI programmable handler), place its logical address in the corresponding level to avoid conflicts with other programmable handlers and also to permit the Resource Manager to assign programmable interrupters to the correct levels. If all interrupters and interrupt handlers are programmable, you can keep the value of `FFh` for all entries in the table.

As part of the hardware capabilities on the GPIB-VXI/C, there are three VXI programmable interrupt handlers. They can be assigned dynamically by the RM or statically according to the contents of the nonvolatile memory.

A24 Assign Base

This entry determines the A24 address where the Resource Manager will begin allocating A24 address space for VXI devices. You can use this field to avoid conflicts with VME devices that use A24 address space. In addition, you can guarantee that a bus master can access the range of address space that a particular device is configured to occupy. The VXIbus specification requires A24 bus masters to see addresses from 200000h to DFFFFFh.

A32 Assign Base

This entry determines the A32 address where the Resource Manager will begin allocating A32 address space for VXI devices. You can use this field to avoid conflicts with VME devices that use A32 address space. In addition, you can guarantee that a bus master can access the range of address space that a particular device is configured to occupy. The VXIbus specification requires A32 bus masters to see addresses from 20000000h to DFFFFFFFh.

DC Starting Logical Address

This parameter specifies the first logical address the Resource Manager should use to begin assigning Dynamic Configuration (DC) devices. DC devices will be assigned the next higher unassigned logical address.

BNO

This parameter specifies whether the Resource Manager should send *Identify Commander* and *Begin Normal Operation* in a DC system. DC systems cannot specify an intended hierarchy and must be configured externally—normally through the local commands `DCGrantDev` and `DCBNOsend`. The most common configuration, however, is to assign all DC devices to Logical Address 0 (the RM). If BNO is specified to be sent, all DC devices are assigned to Logical Address 0 and the *Identify Commander* and *Begin Normal Operation* commands are sent. If BNO is specified *not* to be sent, no devices—neither SC nor DC—will be sent the *Begin Normal Operation* command. `DCBNOsend` must be sent to the local command set to initiate normal operation after the hierarchy is established.

For FAILED Device

The VXIbus specification requires Commanders to Sysfail-Inhibit a Servant device that has failed (asserted the SYSFAIL* line and the Passed bit in its Status register). The specification permits Commanders to also set the reset bit of a failed device. This parameter specifies which method to use.

Servant Area

This parameter specifies what Servant area value to return to the Resource Manager during a Word Serial *Read Servant Area* query. This parameter applies only when the GPIB-VXI/C is not Resource Manager.

GPIB Primary

This parameter specifies the GPIB primary address of the GPIB-VXI/C to be used when in multiple secondary addressing mode.

GPIB Address Assignment Method

This parameter specifies what method to use to configure the GPIB address of the GPIB-VXI/C. The choices are as follows:

- Default:
  - 0 for multiple secondary addressing
  - 1 for multiple primary addressing
- Always a particular GPIB address
- No GPIB address

GPIB Flags

- MultPrimary: Multiple primary addressing mode is set.
- MultSecond: Multiple secondary addressing mode is set.
- Others: These flags are for information purposes only; do not modify.

GPIB Addresses to Avoid

This is a 32-bit bit mask of GPIB addresses to avoid during address assignment for either multiple primary or multiple secondary addressing modes.

Code Instrument Block Base

This parameter specifies the local GPIB-VXI/C address base for Static Code Instruments.

Note National Instruments no longer supports development of Code Instruments.

Code Instrument Number of RAM Blocks

This parameter specifies the number of 4-KB RAM blocks allocated from the block base for use by Static Code Instruments.

Resident Code Instrument Locations

These parameters specify the base addresses of EPROMed Code Instruments. These Code Instruments are automatically started up after the Resource Manager operations complete.

Code Instrument Nonvolatile User Configuration Variables

These parameters are completely user-defined and can be used for any purpose.

Change Configuration Information

The item `Change Configuration Information` displays the GPIB-VXI/C Nonvolatile Configuration Changer as shown.

```
       GPIB-VXI Nonvolatile Configuration Changer
             (C) 1995 National Instruments
================================================
0). Edit Local Register Configuration
1). Edit pSOS Configuration
2). Edit VXI Interrupt Handler Logical Address
3). Edit Resource Manager Configuration
4). Edit Servant Area and DC Configuration
5). Edit FAILED Device Handling Mode
6). Edit GPIB Configuration
7). Edit Default CI Configuration
8). Edit Resident CI Base Locations
9). Edit CI User Configuration Variables
Q). Quit Editor

    Choice (0-9,Q):
```

You can edit the National Instruments-reserved configuration parameters and CI user configuration variables by selecting the corresponding menu item. In each case, you are prompted to enter constants for the new values, with default values supplied where appropriate. For the pSOS configuration parameters, the GPIB-VXI/C prints a formula for calculating an appropriate value for each parameter if you type in 0 in response to the prompt requesting the value.

The Default CI Configuration and Resident CI Base Locations options are only important when installing a Resident CI. Refer to Appendix B, *Using the DMAmove and CDS-852 Adapter Code Instruments*, for instructions on installing the Resident CIs.

Note The Change Configuration Information editor modifies only the RAM copy of the NV memory contents. You must update the NV memory with the `Write Back (Save) Changes` command in the main menu to retain the changes after the GPIB-VXI/C has been reset or powered-down.

Select `Quit Editor` to return the display to the main menu.

Set Configuration to Factory Settings

The item `Set Configuration to Factory Settings` sets the contents of the RAM copy of the NV memory to the default (original) factory settings. Notice that only the RAM copy is affected. You must use the `Write Back (Save) Changes` command in the main menu to write back the NV memory and retain the changes after the GPIB-VXI/C has been reset or powered-down.

Write Back (Save) Changes

The item `Write Back (Save) Changes` writes the modified copy of the NV memory back to the EEPROM. The write-back procedure takes five to 10 seconds.

Quit Configuration

The item `Quit Configuration` prompts you to select a different startup configuration.

5

Diagnostic Tests

This chapter contains information for executing the GPIB-VXI/C diagnostic self-tests. The diagnostics test each GPIB-VXI/C subcircuit and are useful in detecting and isolating problems.

You can enter diagnostics mode through either of the following methods:

- Set the startup mode switches to the diagnostics mode as described in the *GPIB-VXI/C Startup Mode Configuration* section of Chapter 2. For this mode, set switch S19 to the *ON* position and set switch S20 to the *OFF* position. Restart the system.
- In 488-VXI runtime system mode, you can enter the diagnostic mode through the `DIAG` command.

The diagnostic commands must be executed from the RS-232 port.

Configuration for Diagnostic Testing

The diagnostic tests require the GPIB-VXI/C to be disconnected from all other GPIB devices to prevent interference with the GPIB tests.

Diagnostic Test Structure

A total of 263 diagnostic routines, or *tests*, are organized in groups as shown in Table 5-1. Each test is composed of one or more subroutines called *commands*.

Each test is designed to functionally test a specific part of the GPIB-VXI/C circuitry. You can execute the diagnostics by test groups or by individual tests.

Table 5-1. Diagnostic Tests

Test Name	Group Number	Test Numbers	
		From	To
RAM	1	1	4
68070 CPU	2	5	21
MIGA	3	22	44
GPIB	4	45	132
TIC	5	133	236
DMA	6	237	247
68881 Coprocessor	7	248	248
RAM (exhaustive)	8	249	250
Interrupts	9	251	253
Miscellaneous Tests	10	254	263

Diagnostics Mode Selection

Two hierarchical levels of menus control execution of the diagnostic tests. The highest-level menu is the Diagnostics Mode menu, which you can use to select whether to execute a test group or tests, and the mode in which to run them. The Diagnostics Mode menu is shown in the following example and described in Table 5-2.

```
488-VXIbus Interface DIAGNOSTICS:      < XXX DRAM Reported >

     Default Diags(all   ===> d
     Tests               ===> t
     Test Groups         ===> g
     Over NightLoop      ===> o
     Quit                ===> q

PRINT TOGGLE            ===> p
SINGLE STEP TOGGLE      ===> s
LOOPING TOGGLE          ===> l
ERROR REPORT TOGGLE     ===> e
REPORT ERROR LOG        ===> r
CLEAR ERROR LOG         ===> c
(Current settings: PRINT(OFF), ERROR(ON), SINGLE(OFF), LOOP(OFF))

Enter Selection   :
```

Table 5-2. Diagnostics Mode Menu Option Descriptions

Selection	Description
Default Diags (all)	Runs all the tests.
Tests	Presents a menu of tests to be selected.
Test Groups	Presents a menu of test groups to be selected.
Over Night Loop	Runs selected tests continuously. Only stops when an error occurs or when system is reset.
Print Toggle	Turn printing of test groups/tests on or off.
Single Step Toggle	Turns single-stepping of test groups/tests on or off.
Looping Toggle	Turns looping of selected test groups/tests on or off.
Error Report Toggle	Turns printing of error statements on or off.
Report Error Log	Prints the first 11 errors that occurred.
Clear Error Log	Erases the buffer of errors.

By default, single-stepping, looping, and test message printing are turned off while error reporting is turned on. The selected diagnostics run uninterrupted until they complete or until an error occurs. If an error has

occurred, an error message is printed to the screen. The message displays the test number, group number, the value expected, and the value received. Contact National Instruments for further interpretation of diagnostic error messages.

You can suppress the error reporting with the e command. With error reporting turned off, you can select and run tests to completion without being interrupted by error messages. The GPIB-VXI/C informs you if any errors have occurred after all the tests you selected have completed. To view the errors, select `r` to display the error log. Select `c` to clear the error log.

Single Step Toggle is another useful feature you can use to pinpoint problems. Select s to toggle this command on or off. With this feature, each access to memory or to a register is reported on the screen. In addition, the GPIB-VXI/C waits for you to press a key before actually performing the displayed step.

Diagnostic Test Selection

If you select the Default Diags (all) option or the Over Night Loop option, the appropriate tests begin immediately. The default option performs all of the tests, while the Over Night Loop option performs all except the interactive tests and tests that drive signals on the VXIbus. When you select either the Tests or the Test Groups option, a new menu appears from which you can select any or all tests or test groups. The following example shows the Test Selection menu. The Test Group Selection menu is very similar.

```
GROUP              GROUP       TEST NOs
NAME                NUM        FROM - TO
-----------------------------------------
RAM                   1          1  - 4
68070 - I2C           2          5  - 7
68070 - UART          2          8  - 20
68070 - TIMER         2         19  - 21
MIGA                  3         22  - 44
GPIB - NAT4882        4         45  - 99
GPIB - TURBO 488      4        100  - 132
TIC                   5        133  - 236
DMA                   6        237  - 247
MC68881               7        248  - 248
RAM(exhaustive)       8        249  - 250
INTERRUPTS            9        251  - 253
MISC TESTS           10        254  - 263
```

```
ENTER TEST NUMBERS

e.g. : 15,30,31,40-80,99,*(all)
Hit 'q' to quit

Enter:
```

When you have completed all the diagnostic tests, select `q` to quit and exit diagnostics mode. The GPIB-VXI/C prompts you to reboot the system in a different startup mode.

Diagnostic Test Groups

Group 1–RAM

This group tests the RAM to ensure that the CPU can correctly read and write from RAM addresses. Table 5-3 gives the test numbers and names of the RAM tests.

Table 5-3. RAM Tests

Test Number	Test Description
1	Data path test
2	Self-test cell test (not exhaustive)
3	Cell test
4	Read and Modify Write test

Group 2–68070 CPU

This group tests the 68070 I^2C interface, UART interface, and timers. Tests 5 through 7 test the 68070 I^2C interface, tests 8 through 18 test the UART interface, and tests 19 through 21 test the timers. Table 5-4 gives the test numbers and names of the 68070 CPU tests.

Table 5-4. 68070 CPU Tests

Test Number	Test Description
5	I^2C interface test—maximum clock frequency
6	I^2C interface test—maximum clock frequency
7	I^2C interface test—interrupt trigger

Table 5-4. 68070 CPU Tests (Continued)

Test Number	Test Description
8	Test baud rate 75
9	Test baud rate 150
10	Test baud rate 300
11	Test baud rate 1,200
12	Test baud rate 2,400
13	Test baud rate 4,800
14	Test baud rate 9,600
15	Test baud rate 19,200
16	Baud = 9,600; test odd parity with two stop bits
17	Baud = 9,600; test even parity with two stop bits
18	Baud = 9,600; test interrupts
19	Test Timer 0 interrupt capability
20	Test Timer 1 matched mode
21	Test Timer 2 matched mode

Group 3–MIGA

This group tests the MIGA registers. The MIGA, a gate array designed by National Instruments, contains the VXI registers as defined for Message-Based devices. Table 5-5 gives the test numbers and names of the MIGA tests.

Table 5-5. MIGA Tests

Test Number	Test Description
22	Logical address test
23	ID test
24	Device type test
25	Offset test
26	Protocol test

Table 5-5. MIGA Tests (Continued)

Test Number	Test Description
27	A24 Pointer High test
28	A24 Pointer Low test
29	A32 Pointer High test
30	A32 Pointer Low test
31	Data Extended test
32	Data High (device) test
33	Data Low (device) test
34	Data High (local) test
35	Data Low (local) test
36	Status test
37	Constrol test
38	Response test
39	ICR & ISR test
40	I/O test
41	Signal test
42	Interrupts test
43	Word Serial Protocol test
44	SYSFAIL circuitry test

Group 4–GPIB

This group tests the TNT4882 interface IC. Table 5-6 gives the test numbers and names of the GPIB tests.

Table 5-6. GPIB Tests

Test Number	Test Description
45	INIT
46	Presence test using ADSR
47	Check SPMR and SPSR
48	Check address register bits
49	Check can be listener
50	Check can be talker
51	Check can listen to all 32 listen addresses
52	Check can be unaddressed as listener
53	Check can talk to all 32 talk addresses
54	Check can be unaddressed as talker
55	Check can listen to all 960 external addresses
56	Check can be unaddressed as external listener
57	Check can talk to all 960 external addresses
58	Check can be unaddressed as external talker
59	Check can recognize DI and HLDA bits
60	Check can recognize ERR
61	Check can recognize DCL command
62	Check can recognize SDC
63	Check can set END bit on EOI
64	Check can set EOI bit on EOI
65	Check can set END on 8-bit EOS
66	Check can set END on 7-bit EOS
67	Check can recognize GET command

Table 5-6. GPIB Tests (Continued)

Test Number	Test Description
68	Check set APT on unrecognized command
69	Check can recognize undefined command
70	Check can set REM, REMC, LOK, and LOKC bits
71	Check can clear REM and LOK bits
72	Checkk can set SRQI
73	Check can do serial poll
74	Check can do parallel poll
75	Check DHADT
76	Check DHADC
77	Check DHATA
78	Check DHALA
79	Check DHUNTL
80	Check NTNL
81	Check NTNL with ATN asserted
82	Check RPP
83	Check CHES
84	Check PP2
85	Check SDB
86	Check NL
87	Check EOS
88	Check 9914 and 7210 mode switch
89	Check able to untalk
90	Check able to unlisten
91	Check NBAF and NTNL
92	Check REQTC
93	Check REQFC

Table 5-6. GPIB Tests (Continued)

Test Number	Test Description
94	Check holdoff now command
95	Check DHALL
96	Check effect of REQT during serial poll
97	Check for spurious interrupts
98	Check INT on SYNC
99	Check global interrupt
100	Set and clear SC
101	Set and clear DUALADD
102	Trigger INTSCR1 and INTSRC2
103	Set STOP DONE HALT and DAV in read mode
104	Verify set of STS1, ISR3 bits with 8-bit read
105	Verify write mode and TLCINT set by error
106	Read/write CNTL, CNTH registers
107	Verify bits in IMR3 register
108	Reset ISR3
109	Reset ISR3 and STS1
110	Reset STS2
111	Reset TIMER
112	Check flags on 16-bit independent FIFO
113	Fill and empty 16-bit independent FIFO
114	Fill and empty 16-bit FIFO
115	Reset non-full FIFO
116	Reset full FIFO
117	16-bit FIFO read
118	Fill and empty 16-bit FIFO
119	STOP and HALT in 16-bit A-1st mode

Table 5-6. GPIB Tests (Continued)

Test Number	Test Description
120	Holdoff when FIFO and DIR are full
121	HALT and EOI when last byte in FIFO
122	Enable carry cycle
123	Disable carry cycle
124	16-bit FIFO write
125	Fill and empty 16-bit FIFO
126	Carry cycle with EOI
127	Halt on ERROR
128	Interrupt on DONE
129	GPIB → MEMORY DMA
130	GPIB → MEMORY DMA with EOI
131	MEMORY → GPIB DMA
132	MEMORY → GPIB DMA, commands

Group 5–TIC

This group tests the TIC portion of the MANTIS ASIC. The MANTIS, an ASIC designed by National Instruments, handles the TTL/ECL trigger interface and CLK10 conversion. Table 5-7 gives the test numbers and names of the TIC tests.

Table 5-7. TIC Tests

Test Number	Test Description
133	Initialization
134	Register initialization
135	CNTH Register
136	CNTL Register
137	TTCR and TTSR Registers
138	ETCR and ETSR Registers

Table 5-7. TIC Tests (Continued)

Test Number	Test Description
139	MODIDH and MODIDL Registers
140	PGP0 and PGP1 Registers
141	TSR0 and TOR0 Registers
142	TSR1 and TOR1 Registers
143	TSR2 and TOR2 Registers
144	TSR3 and TOR3 Registers
145	TSR4 and TOR4 Registers
146	TSR5 and TOR5 Registers
147	TSR6 and TOR6 Registers
148	TSR7 and TOR7 Registers
149	TSR8 and TOR8 Registers
150	TSR9 and TOR9 Registers
151	GPIN0 connection
152	GPIN1 connection
153	GPIN2 connection
154	GPIN3 connection
155	GPIN4 connection
156	GPIN5 connection
157	GPIN6 connection
158	GPIN7 connection
159	GPIN8 connection
160	GPIN9 connection
161	Trig0 connection
162	Trig1 connection
163	Trig2 connection
164	Trig3 connection

Table 5-7. TIC Tests (Continued)

Test Number	Test Description
165	Trig4 connection
166	Trig5 connection
167	Trig6 connection
168	Trig7 connection
169	Trig8 connection
170	Trig9 connection
171	Counter using CLK10
172	Counter using Trig0
173	Counter using Trig1
174	Counter using Trig2
175	Counter using Trig3
176	Counter using Trig4
177	Counter using Trig5
178	Counter using Trig6
179	Counter using Trig7
180	Counter using Trig8
181	Counter using Trig9
182	Counter using EXT CLK
183	Interrupt on Trig0 by ASTS and USTS
184	Interrupt on Trig1 by ASTS and USTS
185	Interrupt on Trig2 by ASTS and USTS
186	Interrupt on Trig3 by ASTS and USTS
187	Interrupt on Trig4 by ASTS and USTS
188	Interrupt on Trig5 by ASTS and USTS
189	Interrupt on Trig6 by ASTS and USTS
190	Interrupt on Trig7 by ASTS and USTS

Table 5-7. TIC Tests (Continued)

Test Number	Test Description
191	Interrupt on Trig8 by ASTS and USTS
192	Interrupt on Trig9 by ASTS and USTS
193	Interrupt on counter count down on CLK10
194	Interrupt on counter count down on EXTCLK
195	Interrupt AOVER, UOVER, and PSOVER on Trig0
196	Interrupt AOVER, UOVER, and PSOVER on Trig1
197	Interrupt AOVER, UOVER, and PSOVER on Trig2
198	Interrupt AOVER, UOVER, and PSOVER on Trig3
199	Interrupt AOVER, UOVER, and PSOVER on Trig4
200	Interrupt AOVER, UOVER, and PSOVER on Trig5
201	Interrupt AOVER, UOVER, and PSOVER on Trig6
202	Interrupt AOVER, UOVER, and PSOVER on Trig7
203	Interrupt AOVER, UOVER, and PSOVER on Trig8
204	Interrupt AOVER, UOVER, and PSOVER on Trig9
205	Interrupt from scalar
206	Software Semi-Sync accept on Trig0
207	Software Semi-Sync accept on Trig1
208	Software Semi-Sync accept on Trig2
209	Software Semi-Sync accept on Trig3
210	Software Semi-Sync accept on Trig4
211	Software Semi-Sync accept on Trig5
212	Software Semi-Sync accept on Trig6
213	Software Semi-Sync accept on Trig7
214	Software Semi-Sync accept on Trig8
215	Software Semi-Sync accept on Trig9
216	Hardware Semi-Sync and Automatic ACK on Trig0

Table 5-7. TIC Tests (Continued)

Test Number	Test Description
217	Hardware Semi-Sync and Automatic ACK on Trig1
218	Hardware Semi-Sync and Automatic ACK on Trig2
219	Hardware Semi-Sync and Automatic ACK on Trig3
220	Hardware Semi-Sync and Automatic ACK on Trig4
221	Hardware Semi-Sync and Automatic ACK on Trig5
222	Hardware Semi-Sync and Automatic ACK on Trig6
223	Hardware Semi-Sync and Automatic ACK on Trig7
224	Hardware Semi-Sync and Automatic ACK on Trig8
225	Hardware Semi-Sync and Automatic ACK on Trig9
226	Automatic Semi-Sync source
227	Sync triggers with no conditioning
228	Sync triggers with synchronously
229	Pulse stretch synchronous with EXT CLK
230	Pulse stretch with 1CLK synchronous
231	Pulse stretch asynchronously
232	Scalar values 1 through 32 with EXT CLK
233	Scalar value 2 with all GPIO lines
234	Scalar value 0x0f using CLK 10, NOROLL1, and INT
235	TRIGIN and TRIGOUT on front panel
236	TRIGIN and TRIGOUT by zig zag of all triggers

Group 6–DMA

This group tests the DMA Channel 2 and memory-to-memory DMA transfers. Table 5-8 gives the test numbers and names of the DMA tests.

Table 5-8. DMA Tests

Test Number	Test Description
237	Poll test (burst, bytes, mem-to-dev, from even addresses)
238	Poll test (cycle steal, bytes, mem-to-dev, even addresses)
239	Poll test (burst, words, mem-to-dev, from even addresses)
240	Poll test (cycle steal, words, mem-to-dev, even addresses)
241	Poll test (burst, bytes, mem-to-dev, from odd addresses)
242	Poll test (cycle steal, bytes, mem-to-dev, odd addresses)
243	Poll test (burst, bytes, dev-to-mem, from even addresses)
244	Poll test (burst, words, dev-to-mem, from even addresses)
245	DMA interrupt test
246	Minimum functionality test
247	Maximum transfer test

Group 7–68881 Coprocessor

This is a test of the numeric coprocessor operation. If the 68881 is not installed, the GPIB-VXI/C skips this test. Table 5-9 gives the test number and name of the 68881 Coprocessor test.

Table 5-9. 68881 Coprocessor Test

Test Number	Test Description
248	Test floating point coprocessor

Group 8–RAM (Exhaustive)

This exhaustive RAM test checks the entire onboard RAM and the address and data paths. Table 5-10 gives the test numbers and names of the exhaustive RAM tests.

Table 5-10. RAM (Exhaustive) Tests

Test Number	Test Description
249	Data path test (exhaustive)
250	Address path and cell test (exhaustive)

Group 9–Interrupts

This group tests the GPIB and MIGA local interrupts. Table 5-11 gives the test numbers and names of the Interrupt tests.

Table 5-11. Interrupt Tests

Test Number	Test Description
251	Verify interrupt on INT2N using SYSFAIL
252	Verify SYSFAIL disable interrupt
253	Verify interrupt on INT1N using done int

Group 10–Miscellaneous Tests

This group tests the EPROM, EEPROM, Sanity Timer, LEDs, MODID register, Local Bus timeouts, and VXI bus timeout. Table 5-12 gives the test numbers and names of the Miscellaneous tests.

Table 5-12. Miscellaneous Tests

Test Number	Test Description
254	LED test: SYSFAIL and FAILED LED
255	LED test: ACCESS LED
256	LED test: TEST LED
257	LED test: ONLINE LED
258	Switch test: Startup switches (S10, S11, and S12)
259	Local BTO test: Test local bus timeout unit

Table 5-12. Miscellaneous Tests (Continued)

Test Number	Test Description
260	VXI BTO test: Test VXI bus timeout unit
261	Sanity timer test: Test enabled/disabled
262	EPROM checksum test
263	EEPROM stamp and checksum test

A

Using the NI-VISA Code Instrument

This appendix formerly contained an overview of the functions, applications, and implementations of software modules known as Code Instruments (CIs), and presented comparisons and illustrations of GPIB-VXI/C operation with and without CIs. Much of this functionality has been included with the NI-VISA Code Instrument for the GPIB-VXI/C (the *NI-VISA CI*), and this appendix now documents the NI-VISA CI.

CIs are a National Instruments GPIB-VXI/C proprietary feature. A CI is a set of software routines running on the GPIB-VXI/C that the system sees as its own message-based device. An external controller can communicate directly with the CI via a GPIB secondary address. The NI-VISA CI provides an optimized implementation of the VISA instrument control standard running on your GPIB-VXI/C. The NI-VISA software on your system automatically uses this to control VXI devices connected through your GPIB-VXI/C controller.

VISA is the recommended means of controlling a GPIB-VXI/C system. All new GPIB-VXI/C applications should use the NI-VISA API.

Introduction to Programming GPIB-VXI Devices in VISA

The GPIB-VXI makes VXI message-based devices appear as if they are GPIB devices with secondary addresses. This provides an easy transition into VXI for customers with existing GPIB systems, because they can use the same NI-488 API to control both types of instruments. However, this is problematic for VXI register-based devices, because their addresses are not mapped directly into the GPIB system.

Message-Based Access with VISA

For message-based programming, an NI-488 program would typically call `ibdev()` with the VXI device's primary and secondary GPIB addresses to get a handle to the specific device. In VISA, a program calls `viOpen()` with the VXI device's logical address—which is a more natural address

because the device is VXI—to get a handle to it. The simplest and most common GPIB-VXI resource string is "GPIB-VXI::<logical address>::INSTR". Once you have a session to the VXI device, the NI-488 and VISA calls to communicate with the device are very similar.

Register-Based Access with VISA

Because register accesses using the GPIB-VXI involve sending requests to the controller itself (using the local command set), NI-488 programs would use ibdev() with the GPIB-VXI *controller's* primary and secondary GPIB addresses. In VISA, you call viOpen() with the VXI *device's* logical address—*the same method for both message-based and register-based devices*—and VISA handles sending the necessary messages to the controller. For programming the device, the following NI-488 messages and VISA operations are roughly equivalent.

Table A-1. Register-based Programming Messages and Operations

NI-488 Message	VISA Operation
"Laddrs?" or "DLAD?"	viFindRsrc()
"RMentry?" or "DINF?"	viGetAttribute()
"Cmdr?"	viGetAttribute() with VI_ATTR_CMDR_LA
"LaSaddr?"	viGetAttribute() with VI_ATTR_GPIB_SECONDARY_ADDR
"Primary?"	viGetAttribute() with VI_ATTR_GPIB_PRIMARY_ADDR
"WREG" or "A16"	viOut16() with VI_A16_SPACE
"RREG?" or "A16?"	viIn16() with VI_A16_SPACE
"A24"	viOut16() with VI_A24_SPACE
"A24?"	viIn16() with VI_A24_SPACE
"SrcTrig"	viAssertTrigger()

Notice that with the INSTR register access operations `viOut16()` and `viIn16()`, you pass a device-relative offset in the specified address space. This is different from the GPIB-VXI/C local command set, which accepts absolute addresses. If your application currently uses absolute addressing and you do not want to convert to device-relative offsets, you may consider the MEMACC resource, which accepts absolute addressing. The form of the resource string for that class is `"GPIB-VXI<system>::MEMACC"`. You also can use the operations `viOut8()` and `viIn8()` to perform 8-bit accesses, which is not a feature supported by the local command set. VISA also defines 32-bit operations and accesses to A32 space, but because these are not implemented by the GPIB-VXI/C itself, they return errors.

DMAmove and VISA

If you have used the `DMAmove` code instrument in the past, you can use the `viMoveInxx()` and `viMoveOutxx()` operations instead. Refer to Appendix B, *Using the DMAmove and CDS-852 Adapter Code Instruments*, for more information. They make use of the GPIB-VXI's DMA functionality but require only a single operation call, instead of the multiple calls required to send the command and data blocks and then poll waiting for the operation to complete. Using VISA to move blocks of data also means that you no longer need to load the `DMAmove` code instrument, as NI-VISA automatically downloads a separate code instrument (the NI-VISA CI) to handle these and other operations. NI-VISA is the recommended way to do DMA with the GPIB-VXI.

Additional Programming Issues

For advanced users, the GPIB-VXI Mainframe Backplane resource encapsulates the operations and properties of each mainframe (or chassis) in a VXIbus system. This resource type lets a controller query and manipulate specific lines on a specific mainframe in a given VXI system. The form of the resource string for this class is "`GPIB-VXI<system>::BACKPLANE`". Services in this resource class allow the user to map, unmap, and assert hardware triggers, and also to assert various utility signals.

Refer to the *NI-VISA User Manual* and the *NI-VISA Programmer Reference Manual* for more information about using NI-VISA and the subset of NI-VISA supported on the GPIB-VXI.

If you have more than one GPIB-VXI controller in your system, or if you change the primary address of a GPIB-VXI controller from its default (1 for the National Instruments GPIB-VXI/C), or if you have a GPIB-VXI controller from another vendor, then you need to configure NI-VISA to find such a controller. Use the NI-VISA configuration utility—MAX on Windows, `visaconf` on UNIX—and explicitly add a GPIB-VXI controller. You will be prompted for the GPIB controller number to which the GPIB-VXI is connected (usually 0), a unique GPIB-VXI controller number, which you are free to assign, and the primary and secondary addresses to which you have configured this GPIB-VXI controller.

GPIB-VXI Summary

In summary, using VISA and the NI-VISA CI to program VXI devices controlled by a GPIB-VXI is the fastest, easiest, and highest performance way to develop and deploy your GPIB-VXI application. Although porting the code from NI-488 to VISA is not simple in the case of register-based programming, it will be high-performance code that is compatible with native VXI controllers.

B

Using the DMAmove and CDS-852 Adapter Code Instruments

This appendix contains instructions for installing and using the National Instruments-supplied Code Instruments (CIs). Two CIs come standard in the firmware of the GPIB-VXI/C. The first CI is called the *DMAmove* CI and is used for dedicating one of the GPIB-VXI/C GPIB addresses for use as a high-speed memory port. The second CI is used for controlling one or more Colorado Data Systems (CDS) 73A-852 adapter modules.

Note The NI-VISA CI is the recommended way to perform DMA with your GPIB-VXI.

The main purpose of the GPIB-VXI/C is to convert GPIB protocols to VXI protocols. However, many features within the VXI environment are not possible with GPIB. Much of this has to do with the memory-mapping architecture of VXI. The DMAmove CI gives you very fast and direct access to VXI A16 and A24 memory, as well as to local GPIB-VXI/C memory. The 68070 DMA channel 2 is used within the DMAmove CI to move data around much more quickly than the VXI Word Serial protocol or individual peeks and pokes.

The 73A-852 is a non-VXI device with communication registers located in A24 space rather than in A16 space. To communicate with the 852 adapter as a Message-Based device, the 73A-852 requires special adapter software. The GPIB-VXI/C performs the Message-Based-to-852 communication translation with a CI. The GPIB-VXI/C firmware release includes one CDS-852 Position Independent CI. This CI implements the configuration and translation functions required to communicate with up to 12 CDS-852 adapter modules via the GPIB.

Using EPROMed Code Instruments

This section discusses how to install, execute, and delete an EPROMed Code Instrument.

Installing an EPROMed Code Instrument

You can install an EPROMed Code Instrument (the DMAmove and CDS-852 CIs are examples) either by configuring the nonvolatile configuration parameters or by using the GPIB-VXI/C local command set command `ECIboot?`. This section explains how to use the

GPIB-VXI/C local command set command `ECIboot?`. This section explains how to use the nonvolatile configuration editor to permanently install an EPROMed Code Instrument.

Enter the nonvolatile configuration mode as described in Chapter 4, *Nonvolatile Configuration*. The following menu is displayed:

```
        GPIB-VXI Nonvolatile Configuration Main Menu
               (C) 1995 National Instruments
    ================================================
    1). Read In Nonvolatile Configuration
    2). Print Configuration Information
    3). Change Configuration Information
    4). Set Configuration to Factory Settings
    5). Write Back (Save) Changes
    6). Quit Configuration

        Choice (1-6):
```

Enter `3` to change the configuration information. The following menu then displays:

```
        GPIB-VXI Nonvolatile Configuration Changer
               (C) 1995 National Instruments
    ================================================
    0). Edit Local Register Configuration
    1). Edit pSOS Configuration
    2). Edit VXI Interrupt Handler Logical Address
    3). Edit Resource Manager Configuration
    4). Edit Servant Area and DC Configuration
    5). Edit FAILED Device Handling Mode
    6). Edit GPIB Configuration
    7). Edit Default CI Configuration
    8). Edit Resident CI Base Locations
    9). Edit CI User Configuration Variables
    Q). Quit Editor

        Choice (0-9,Q):
```

Enter `1` to edit pSOS configuration. The following prompt then appears:

```
------pSOS Configuration------
Enter Dynamic RAM Region 1 Size (default 0x70000):
Enter <CR> to keep the present value and continue to the next entry:
Enter Maximum Number of Processes (default 0x20):
```

The following formula calculates the maximum number of processes:

Number of processes = 10h + (number of GPIB address links) + (2* number of CIs)

If fewer than six CIs are installed and no other GPIB address links exist, the default value of 32 (0x20) is adequate. Increasing the number of processes affects the throughput of the GPIB-VXI/C. Enter the number of processes in hexadecimal.

The next prompt is then displayed:

```
Enter Maximum Number of Exchanges (default 0x20):
```

The following formula calculates the maximum number of exchanges:

Number of exchanges = 10h + (number of CIs)

The default value of 32 (0x20) is adequate even if all 12 CIs are installed. Enter <CR> to select the default value.

The last prompt appears:

```
Enter Maximum Number of Message Buffers (default 0x180):
```

The following formula calculates the maximum number of message buffers:

Number of message buffers = 100h + (25* number of CIs)

If fewer than six CIs are installed, the default value of 384 (180h) is adequate. Increasing the number of message buffers affects the throughput of the GPIB-VXI/C. Enter the number of message buffers in hexadecimal.

When the edit menu reappears, enter 8 to edit the resident CI base locations.

For the DMAmove Code Instrument, only one CI should be created. Configure a single CI base location as shown below. For the CDS-852 adapter, configure as many CI base locations as there are 852 adapters to be controlled by the GPIB-VXI/C. For example, to control four 73A-852s, configure CI base locations 0 through 3. The addresses for the two CIs are as follows.

Code Instrument	Address (Base Location)
CDS852 CI	F7E000
DMAmove CI	F7C000

Type `Y` to respond yes to the `Debug mode On for Resident CI 0xXX` prompt. This enables debug statement printing to the terminal.

For example, to install the single DMAmove CI and two 852 adapter CIs and enable debug statement printing on the second 852 CI, enter the following sequence, which has been highlighted in boldface type for this example:

```
----- Resident CI Base Location Configuration -----
Enter Number of Base Location to EDIT (0xff = EXIT): 0
Enter Address for Base 0x01 (default = 0x000000): F7C000
Debug mode ON for Resident CI 0x01 (default NO): N
Enter Number of Base Location to EDIT (0xff = EXIT): 4
Enter Address for Base 0x00 (default = 0x000000): F7E000
Debug mode ON for Resident CI 0x00 (default NO): <CR>
Enter Number of Base Location to EDIT (0xff = EXIT): 5
Enter Address for Base 0x01 (default = 0x000000): F7E000
Debug mode ON for Resident CI 0x01 (default NO): Y
Enter Number of Base Location to EDIT (0xff = EXIT): <CR>
```

When the edit menu reappears, enter `Q` to exit the configuration editor. When the Nonvolatile Configuration main menu appears, enter `5` to save the configuration changes. When the Nonvolatile Configuration main menu reappears, enter `2` to confirm the configuration information. The CI configuration for the previous example would be displayed as follows:

```
------ Resident Code Instrument Locations ------
0x00: 00F7C000 0x01: 00000000 0x02: 00000000
0x03: 00000000 0x04: 00F7E000 0x05: 00F7E000
0x06: 00000000 0x07: 00000000 0x08: 00000000
0x09: 00000000 0x0A: 00000000 0x0B: 00000000
```

When the main menu reappears, enter `6` to quit the configuration mode. The following message appears:

```
Must Re-initialize pROBE or reboot for pSOS changes to take effect.
Other changes made automatically when configuration saved.

*********************************************
*           DONE WITH CONFIGURATION          *
* Change startup mode Dip settings to enter  *
* different mode or push RESET to reconfigure. *
*********************************************
```

Executing an EPROMed Code Instrument

If a CI is configured in nonvolatile configuration to be executed, the CI will be *booted* upon the next power cycle of the GPIB-VXI/C. The CI booting procedure actually occurs after the Resource Manager has run and the local command set has been initiated on all ports. This guarantees the CI access to all resources of the GPIB-VXI/C.

Deleting a CI

To delete a CI, follow the installation procedure but set the CI's base address location to 000000. If you wish to delete the CI during runtime, after the CI has already been started up, you can use the local command set command, `CIDelete?`.

The DMAmove Code Instrument

After the nonvolatile configuration is complete and the GPIB-VXI/C is rebooted, the DMAmove Code Instrument will be up and running. You should see the following message printed on the serial port:

```
National Instruments' DMAmove Code Instrument Running
```

The following sections describe the runtime capabilities of the DMAmove Code Instrument.

GPIB Address Assignment

The DMAmove CI is assigned Logical Address 160 by default. If a device already exists at Logical Address 160, the DMAmove CI is assigned the next highest available logical address. The GPIB address is assigned to be the upper five bits of the logical address (GPIB address 20), if available. If that GPIB address is taken, it takes the next highest available GPIB address. You can use the local command set command `LaSaddr?` to determine the GPIB address and the local command set command `LaSaddr` to change the GPIB address. You can communicate directly with the DMAmove CI through this GPIB address.

Capabilities and Operation

The DMAmove CI is a Code Instrument built on top of the function `DMAmove()`. As such, the DMAmove CI has all of the capabilities of the `DMAmove` function plus a few extra device interface type features. The following is the C language prototype for the `DMAmove()` function:

```
DMAmove(source, dest, count, mode)

uint32 source     Local address to transfer from
uint32 dest       Local address to transfer to
uint32 count      Number of bytes to transfer
```

`uint32 mode` Bit vector for mode of transfer

- Bit 0: Transfer direction
  - 0 = Source to destination
  - 1 = Destination to source
- Bit 1: Destination size
  - 0 = 16 bit
  - 1 = 8 bit
- Bit 2: Operand size
  - 0 = 16 bit
  - 1 = 8 bit
- Bit 3: DMA transfer mode
  - 0 = Cycle steal
  - 1 = Burst
- Bit 4: Source address increment
  - 0 = Increment source address by operand size
  - 1 = Do not increment source address
- Bit 5: Destination address increment
  - 0 = Increment destination address by destination size
  - 1 = Do not increment destination address

The interface for the DMAmove CI is almost identical. To control the DMAmove CI, simply send 16 binary bytes of information over the GPIB with EOI on the last byte corresponding to the four 32-bit parameters in the `DMAmove` function prototype. The only exception to this for the DMAmove CI is that the value of zero (0) in the `source` parameter specifies to take data from the GPIB as input and the value of zero (0) in the `dest` parameter specifies for the source data to be transmitted out the GPIB. You may not specify zero in both `source` and `dest` parameters. If you are writing data with GPIB as the source, simply follow the 16-byte transfer, which has EOI on the last byte, with the continuous data transfer with EOI on the last byte. If you are reading data from the GPIB-VXI/C out to the GPIB, simply follow the 16-byte transfer, which has EOI on the last byte, with a GPIB read. If both `source` and `dest` are non-zero, the transfer will take place without further action. When either `source` or `dest` is non-zero it specifies a local GPIB-VXI/C address as shown in Figure 5-1.

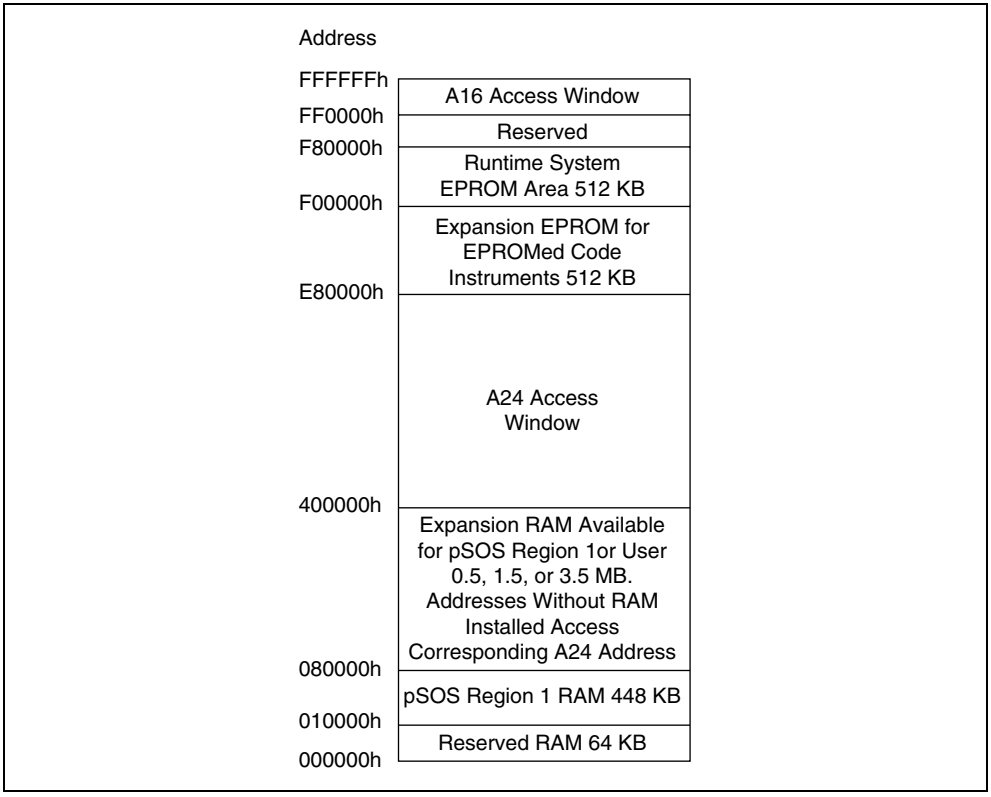


Figure 5-1. GPIB-VXI/C Local Memory Map

You can use the DMAmove CI to perform any of the capabilities of the `DMAmove` function including moving to or from VXI A16 space, VXI A24 space, or local GPIB-VXI/C memory. It can transfer 8- or 16-bit quantities from either source or destination (they can be different). It can increment or not increment addresses as it counts to give fast access to FIFO registers or block memory.

The DMAmove CI reports current status and errors via its status byte and the REQT signal (GPIB SRQ line). The following is a list of the status bytes returned by the DMAmove CI and their corresponding meanings.

Status Value	Meaning
00h	Idle, no operation pending
80h	Operation underway
41h (RSV pending)	DMA timing error
42h (RSV pending)	Bus Error at source
44h (RSV pending)	Bus Error at destination
48h (RSV pending)	Unknown error
50h (RSV pending)	Error in parameter sent

In addition, if Debug mode is specified when the DMAmove CI is booted, diagnostic messages are printed to the serial port. Every access to the DMAmove CI causes messages to be printed. All accesses to or from the GPIB and VXI are logged to the serial port.

The CDS-852 Adapter Code Instrument

After the nonvolatile configuration is complete and the GPIB-VXI/C is rebooted, the CDS-852 Adapter Code Instrument will be up and running. You should see the following message printed on the serial port:

```
National Instruments' CDS 73A-852 Code Instrument Adapter Running
```

The following sections describe the runtime capabilities of the CDS-852 Adapter Code Instrument.

Logical Address and A24 Address Assignment

The 852 adapter CIs are assigned logical addresses sequentially, starting with the lowest configured CI base address and Logical Address 80. For example, if the CIs at base address locations 1 and 3 are installed, the CI at location 1 is assigned Logical Address 80, and the CI at location 3 is assigned Logical Address 81.

The default offset where the CI expects to find its 73A-852 registers in VXI/VME A24 space is related to the CI's logical address as follows:

73A-852 A24 offset = CI logical address * 10000h

For example, a CI at Logical Address 80h expects (by default) to find its 73A-852 registers at offset 800000h. The CI's A24 offset can be changed with the CI command `!!L`. The 73A-852 has rotary switches for changing its A24 register locations.

852 Adapter CI Commands

The 852 adapter CI commands are interpreted by the CI itself and do not directly affect the 852 module. If the adapter CI receives a word serial buffer that does not begin with the `!!` character sequence, it assumes that the buffer is for the 73A-852 and writes the buffer to the appropriate A24 register location. The CI command formats were designed to minimize the possibility of conflict with the command sets of the various plug-in instruments that are compatible with the 852 adapter. Because National Instruments has not had the opportunity to study the command sets of all CDS plug-in instruments, you need to keep in mind the possibility of conflict as you develop your applications.

The `!!A` and `!!B` commands set the CI read mode for compatibility with the CDS instrument. Some CDS command responses are in ASCII format, while others are in binary format. Refer to the appropriate CDS manual for the response format of a particular command. The `!!A` command sets the adapter CI mode to be compatible with the ASCII response format. If the expected response format is binary, use the `!!B` command to set the CI to the binary read mode.

Two termination conditions can apply to reading data from the 73A-852. Depending upon the 73A-852 configuration and the operation being performed, the 852 may terminate the transmission of data with an end-of-string (EOS) character, or it may assert the END bit (VMEbus data bit 8).

The `!!E`, `!!T`, and `!!t` commands configure the CI termination conditions. The EOS and END bit termination conditions are independent; that is, you can configure the CI to terminate a read from the 73A-852 on one condition, both conditions, or neither condition. In addition, you can limit the maximum size of binary mode reads with the `!!S` command. Notice that with binary responses, there can be no unique EOS character, so you should use the END or transfer size conditions (not EOS) to terminate binary transfers. The default read mode is ASCII. The default read termination condition is the EOS character <LF> (0Ah) with the END bit set.

The `!!Q` command returns information about the CI settings (always to the serial port). The `!!D` and `!!d` commands control the printing of runtime debug information to the terminal connected to the serial port.

!!A

Purpose

Set the adapter CI read mode to ASCII, for compatibility with the CDS instrument response.

Command Syntax

```
!!A
```

or

```
!!a
```

Action

Sets the adapter CI read mode to ASCII. The maximum ASCII response size allowed is 512 bytes.

!!B

Purpose

Set the adapter CI read mode to binary.

Command Syntax

```
!!B
```

or

```
!!b
```

Action

Sets the adapter CI read mode to binary. Read size is limited to 512 bytes, or as configured by the `!!S` command.

!!D

Purpose

Enable debug message printing to the serial port.

Command Syntax

```
!!D
```

Action

Enables debug message printing to the serial port.

!!d

Purpose

Disable debug message printing to the serial port.

Command Syntax

```
!!d
```

Action

Disables debug message printing to the serial port.

!!E

Purpose

Configure CI read termination on an EOS character.

Command Syntax

```
!!E <hex number>
```

or

```
!!e <hex number>
```

<hex number> is the ASCII value corresponding to the desired EOS character—for example, 0Ah for <LF).

Action

Enables read termination on an EOS with a value of <hex number>.
If <hex number> is greater than FFh, the EOS termination condition is disabled.

Examples

Set the EOS character to <CR>

```
!!E 0D
```

Disable EOS read termination.

```
!!E 100
```

!!L

Purpose

Set the A24 base address where the adapter CI expects to find the 852 adapter.

Command Syntax

```
!!L <val>
```

or

```
!!l <val>
```

<val> is a hex value equal to the upper 8 bits of the target adapter's A24 address.

Action

The adapter CI expects to find the target 852 adapter at offset <val> * 10000h.
The default (initial) value of <val> is the adapter DCI's logical address.

Example

Set the adapter CI to operate with a 852 adapter at A24 base address 830000h.

```
!!L 83
```

!!S

Purpose

Set the maximum size of a binary read.

Command Syntax

```
!!S <size>
```

or

```
!!s <size>
```

`<size>` is a decimal value.

Action

Sets the maximum binary read size to `<size>` bytes. The default value of the read size is 512 bytes.

!!T

Purpose

Enable read termination when the END bit is set.

Command Syntax

```
!!T
```

Action

Enables read termination when the END bit (bit 8) is set.

!!t

Purpose

Disable read termination on the END bit.

Command Syntax

```
!!t
```

Action

Disables read termination on the END bit (bit 8).

C

Specifications

This appendix lists various module specifications of the GPIB-VXI/C, such as physical dimensions and power requirements.

CPU

Microprocessor..... 16-MHz 68070

Coprocessor (optional)..... 16-MHz 68882

RAM..... 4 MB (configured to use 512 KB)

Physical

C-size VXIbus board
slot requirements..... 1 slot

Local bus keying ..... Class 1, TTL

Front panel indicators

- SYSFAIL ..... red
- FAILED ..... red
- TEST..... green
- ON LINE..... green
- ACCESS ..... yellow

Front panel connectors

- RS-232
- GPIB
- Trigger input
- Trigger output
- External 10-MHz clock

Reset pushbutton

Power Requirements

Source	Typical	Direct Current (max)	Dynamic Current (max)
+5.0 VDC	TBD	TBD	Not Available
+12.0 VDC	TBD	TBD	Not Available
−12.0 VDC	TBD	TBD	Not Available
−5.2 VDC	TBD	TBD	Not Available
−2.0 VDC	TBD	TBD	Not Available

Cooling Requirements

Power dissipation, max.....TBD

Operating Environment

Temperature.....0 to 55 °C

Relative humidity .....0 to 95%, noncondensing

Storage Environment

Temperature.....–40 to 125 °C

Relative humidity .....0 to 100%, noncondensing

EMI

FCC.....Class A verified

Functionality

IEEE-488

Capability Code	Description
SH1	Source Handshake
AH1	Acceptor Handshake
T5, TE5	Talker, Extended Talker

Capability Code	Description
L3, LE3	Listener, Extended Listener
SR1	Service Request
DC1	Device Clear
DT1	Device Trigger
RL0	Remote Local
PP0	Parallel Poll

VXIbus Master/Slave

- A16/A24 Addressing
- A32 Addressing (slave only)
- D08(EO)/D16 Data Paths
- Read-Modify-Write

VXIbus

- VXIbus System Specification Compatible
- Multimainframe Resource Manager (defeatable)
- Slot 0 Support (defeatable)
- Message-Based Commander and Servant
- Dynamically Configurable
- Programmable Handler (any three of seven levels)
- Trigger Source/Acceptor (SYNC, SEMI-SYNC, ASYNC, STST protocols)
- External Trigger I/O Support
- External CLK10 I/O Support

D

Connectors

This appendix describes the connectors found on the GPIB-VXI/C.

Note The illustrations in this appendix show the mating face of the connectors. An asterisk suffix (*) on a signal name indicates that the signal is active low.

RS-232

Connector Type: 9-pin Subminiature D HD-20

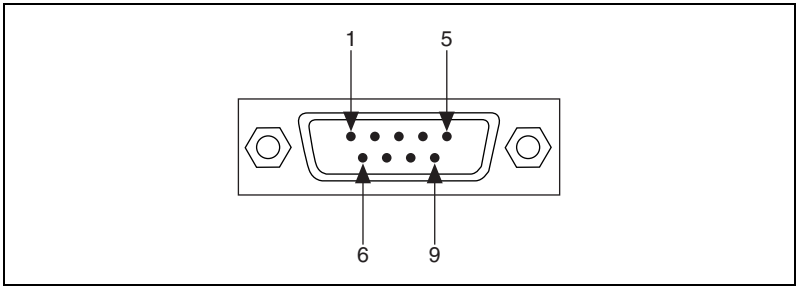


Figure D-1. RS-232 Connector

Table D-1. RS-232 Connector Signals

Pin	Signal Name	Signal Description
1	DFI1	Discrete Fault Indicator (leave unconnected)
2	RXD*	Receive Data
3	TXD*	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	Ground
6	DFI2	Discrete Fault Indicator (leave unconnected)
7	RTS*	Ready to Send

Table D-1. RS-232 Connector Signals (Continued)

Pin	Signal Name	Signal Description
8	CTS	Clear to Send
9	n.c.	Not Connected

Caution If you are building a cable for the RS-232 port, do *not* connect to pins 1 and 6. Connecting to these pins can result in damage to the GPIB-VXI/C. You should connect to these pins only if you are using DFI. Refer to the *Discrete Fault Indicator Configuration* section of Chapter 2, *Configuration and Startup Procedures*, for more information about DFI.

GPIB

Connector Type: GPIB

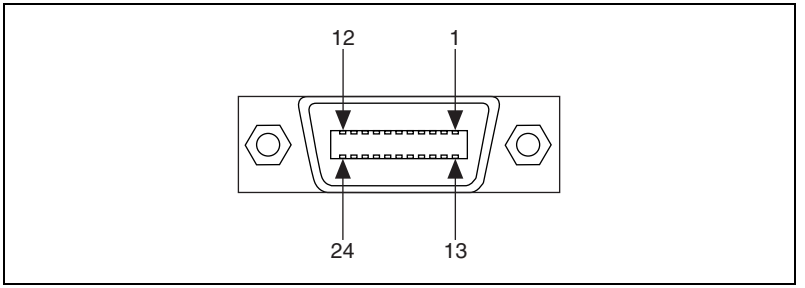


Figure D-2. GPIB Connector

Table D-2. GPIB Connector Signals

Pin	Signal Name	Signal Description
1	DIO1*	Data Bit 1
2	DIO2*	Data Bit 2
3	DIO3*	Data Bit 3
4	DIO4*	Data Bit 4
5	EOI*	End or Identify
6	DAV*	Data Valid
7	NRFD*	Not Ready for Data

Table D-2. GPIB Connector Signals (Continued)

Pin	Signal Name	Signal Description
8	NDAC*	Not Data Accepted
9	IFC*	Interface Clear
10	SRQ*	Service Request
11	ATN*	Attention
12	SHIELD	Chassis ground
13	DIO5*	Data Bit 5
14	DIO6*	Data Bit 6
15	DIO7*	Data Bit 7
16	DIO8*	Data Bit 8
17	REN*	Remote Enable
18	GND	Logic Ground
19	GND	Logic Ground
20	GND	Logic Ground
21	GND	Logic Ground
22	GND	Logic Ground
23	GND	Logic Ground
24	GND	Logic Ground

External CLK10

Connector Type: BNC

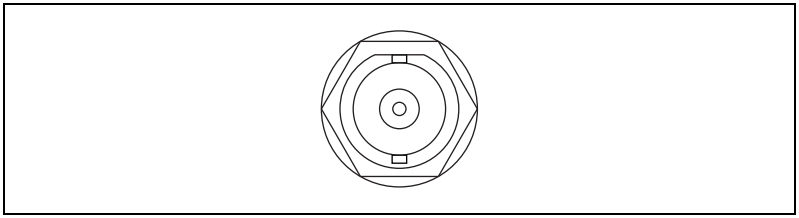


Figure D-3. EXT CLK Connector

Table D-3. EXT CLK Connector Signals

Pin	Signal Description
Center	CLK10 I/O (TTL, 10 MHz)
Shield	Ground

Trigger Input

Connector Type: BNC

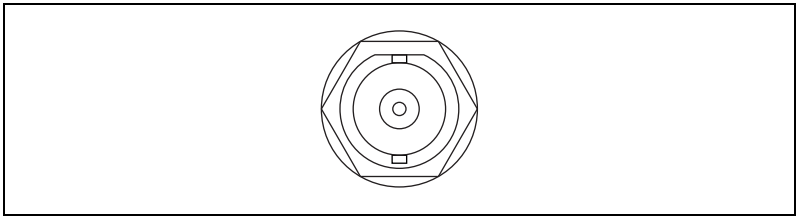


Figure D-4. TRG IN Connector

Table D-4. TRG IN Connector Signals

Pin	Signal Description
Center	Trigger Input (TTL)
Shield	Ground

Trigger Output

Connector Type: BNC

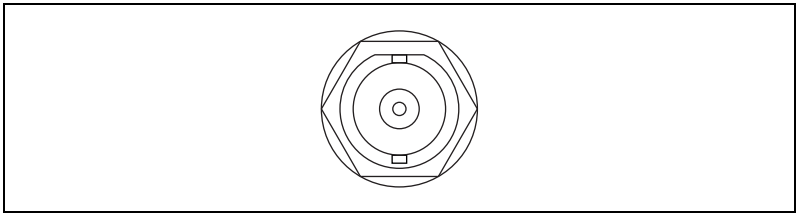


Figure D-5. TRG OUT Connector

Table D-5. TRG OUT Connector Signals

Pin	Signal Description
Center	Trigger Output (TTL, 50Ω driver)
Shield	Ground

VXIbus P1 and P2

Connector Type: 96-pin DIN

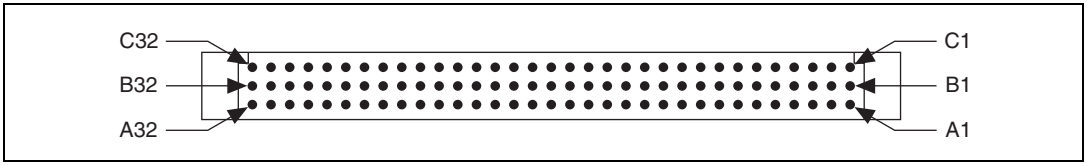


Figure D-6. VXIbus Connector

Table D-6. VXIbus P1 Connector Signals

Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	not connected	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12

Table D-6. VXIbus P1 Connector Signals (Continued)

Pin	Row A	Row B	Row C
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	not connected	A17
22	IACKOUT*	not connected	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08

Table D-6. VXIbus P1 Connector Signals (Continued)

Pin	Row A	Row B	Row C
31	–12 V	not connected	+12 V
32	+5 V	+5 V	+5 V

Table D-7. VXIbus P2 Connector Signals

Pin	Row A	Row B	Row C
1	ECLTRG0	+5 V	CLK10+
2	–2 V	GND	CLK10–
3	ECLTRG1	not connected	GND
4	GND	A24	–5.2 V
5	MODID12	A25	LBUSC00
6	MODID11	A26	LBUSC01
7	–5.2 V	A27	GND
8	MODID10	A28	LBUSC02
9	MODID09	A29	LBUSC03
10	GND	A30	GND
11	MODID08	A31	LBUSC04
12	MODID07	GND	LBUSC05
13	–5.2 V	+5 V	–2 V
14	MODID06	not connected	LBUSC06
15	MODID05	not connected	LBUSC07
16	GND	not connected	GND
17	MODID04	not connected	LBUSC08
18	MODID03	not connected	LBUSC09
19	–5.2 V	not connected	–5.2 V
20	MODID02	not connected	LBUSC10
21	MODID01	not connected	LBUSC11

Table D-7. VXIbus P2 Connector Signals (Continued)

Pin	Row A	Row B	Row C
22	GND	GND	GND
23	TTLTRG0*	not connected	TTLTRG1*
24	TTLTRG2*	not connected	TTLTRG3*
25	+5 V	not connected	GND
26	TTLTRG4*	not connected	TTLTRG5*
27	TTLTRG6*	not connected	TTLTRG7*
28	GND	not connected	GND
29	not connected	not connected	not connected
30	MODID00	not connected	GND
31	GND	GND	+24 V
32	SUMBUS	+5 V	–24 V

E

Error Codes

This appendix lists the local command set error codes and describes the error associated with each error code.

Table E-1. Error Codes

Error Number	Type	Description
0	Format	Command format error
1	Syntax	Command was not found
2	Syntax	Illegal identifier after <Program Data Separator>
3	Syntax	Missing <Program Data Separator>
4	Syntax	Maximum <Program Mnemonic> length is 12 characters
5	Syntax	Illegal command: Expecting upper or lower case alpha
6	Syntax	Illegal command
7	Syntax	Illegal non-numeric
8	Syntax	Illegal <Decimal Numeric Program Data>
9	Syntax	Illegal <Suffix Program Data>
10	Syntax	Maximum <Suffix Program Data> length is 12 characters
11	Syntax	Illegal <String Program Data>
12	Syntax	Illegal <Arbitrary Block Program Data>
13	Syntax	Illegal <Expression Program Data>
14	Syntax	Illegal <Character Program Data>
15	Syntax	Illegal character on input
16	Syntax	Illegal identifier after command
17	Syntax	Illegal identifier after <Program Separator>

Table E-1. Error Codes (Continued)

Error Number	Type	Description
18	Syntax	Missing `<Program Separator>`
19	Syntax	Too much data
30	Device	No error
31	Device	Logical address is out of range 0 through 254
32	Device	No device is at that logical address
33	Device	GPIB secondary address is out of range 0 through 30
34	Device	VXI interrupt handler number is out of range 1 through 3
35	Device	VXI interrupt level is out of range 0 through 7
36	Device	A16 address is out of range 0000h through FFFEh
37	Device	Address must be even
38	Device	Word write value is out of range 0000h through FFFFh
39	Device	A bus error occurred during the access
40	Device	A24 address is out of range 200000h through E7FFFEh
41	Device	488.2 register is out of range 0 through 255
42	Device	Console mode is disabled: must have one output mode enabled
43	Device	Logical device has no secondary address link
44	Device	Unable to delete secondary address link
45	Device	Unable to create secondary address link
46	Device	Secondary address is already attached to a logical address
47	Device	Device is not a Message-Based device
48	Device	Device is not a servant of this GPIB-VXI/C
49	Device	Device does not have commander capability
50	Device	Not Dynamically Configured
51	Device	Commander did not accept *Device Grant* command
52	Device	Servant did not accept BNO or *Identify Commander* command

Table E-1. Error Codes (Continued)

Error Number	Type	Description
53	Device	Logical address cannot be this GPIB-VXI/C
54	Device	Word Serial command is out of range 0 through FFFFh
55	Device	Logical address is not physical VXI device
56	Device	Unable to create I/O buffer
57	Device	Commander did not accept *Release Device* command
58	Device	Unable to grant CI to physical device
59	Device	Device is already a servant
60	Device	Device is not commander of servant
61	Device	Register offset out of range 0 through 3Eh
62	Device	Timeout waiting for Downloaded Data
63	Device	TTL/ECL trigger line out of range 0 through 9
100	CI	DCI functionality is inactive
101	CI	Logical address conflict
102	CI	Logical address is out of range
103	CI	Block(s) requested are used
104	CI	Block(s) requested do not exist
105	CI	Servant(s) requested do not exist
106	CI	Servant(s) requested are not servants of the GPIB-VXI/C or another DCI
107	CI	Commander requested does not exist
108	CI	Servant(s) requested do not have the same commander
109	CI	Requested zero blocks
110	CI	Logical address referenced is not a DCI
111	CI	DCI base address is out of range
112	CI	DCI area new base address is not a multiple of 4,096

Table E-1. Error Codes (Continued)

Error Number	Type	Description
113	CI	DCI area request exceeds available memory
114	CI	Attempted to change DCI area while DCIs were installed
116	CI	DCI was not found
117	CI	Logical address referenced is not a DCI
120	CI	Error encountered while spawning DCI process(es)
121	CI	Error encountered while creating Asynch process exchange
122	CI	No DCI initialization information; need to do `DCISetup?` query
123	CI	Download timed out
125	CI	Download overflowed requested blocks
126	CI	Servant(s) requested has secondary address link
127	CI	Memory requested for DCI Word Serial structures is unavailable
128	CI	Logical address referenced is not the GPIB-VXI/C or local DCI
129	CI	Logical address referenced is not GPIB-VXI/C's or CI's servant
130	CI	Stack size requested for worker process exceeds FFFFh words
301	Trigger	No Trigger hardware support for this operation
302	Trigger	Invalid Controller for trigger functions
303	Trigger	Invalid Trigger line, External line, or protocol
304	Trigger	Trigger line not supported
305	Trigger	Trigger protocol not supported
306	Trigger	Wait period exceeded, timeout occurred
307	Trigger	Line already configured; must unconfigure to configure
308	Trigger	Source line not supported
309	Trigger	Destination line not supported for this source
310	Trigger	Invalid configuration mode
311	Trigger	Line already mapped; must unmap to map

Table E-1. Error Codes (Continued)

Error Number	Type	Description
312	Trigger	Line has not been configured/mapped for this operation
313	Trigger	Invalid count (TICK = 0 through 32, CNTR = 0 through 65,535)
314	Trigger	Invalid/Unsupported mapping signal conditioning mode
315	Trigger	Previous operation is still pending for this line
316	Trigger	Previous acknowledge is still pending for this line
33064	Trigger	Trigger overrun, too many triggers received
33068	Trigger	Trigger unassertion overrun, too many triggers received
33076	Trigger	Trigger pulse stretch overrun, too many triggers received

F

GPIB-VXI/C VXI Trigger Support

This appendix contains an overview of the VXI triggering capabilities of the GPIB-VXI/C.

The GPIB-VXI/C contains a custom ASIC designed by National Instruments called the MANTIS. The MANTIS gives direct access/control to the VXI trigger lines as well as some unique hardware features such as a 16-bit counter/timer, a dual 5-bit tick timer, and a 10 by10 crosspoint switch matrix. It also includes some minimal signal conditioning such as signal inversion, variable pulse stretching, and synchronization with a clock source. The MANTIS supports all VXI-defined trigger protocols on the eight VXI TTL trigger lines and the two P2 connector ECL trigger lines.

In addition, the MANTIS has 10 external connections referred to as General Purpose Input/Output (GPIO) connections. Figure F-1 shows the configuration of the GPIOs on the GPIB-VXI/C. You can route a GPIO to any or all of the VXI trigger lines or the 5-bit tick timer. By using the built-in 10 MHz clock or GPIO 13.975 kHz, 4.9152 MHz, or TRIG IN connections, you can generate a square wave on any or all of the backplane trigger lines. By using the dual 5-bit tick timers, you can divide any of these frequencies down to a lower frequency. You can also disconnect a GPIO from its external connection and use it as a crosspoint switch location. In this mode, you can use any single trigger line as the internal source for the GPIO and any or all of the remaining trigger lines as the destination.

Refer to the *TTL/ECL Trigger Access Commands* section of Chapter 3, *Local Command Set*, for information on programming the MANTIS.

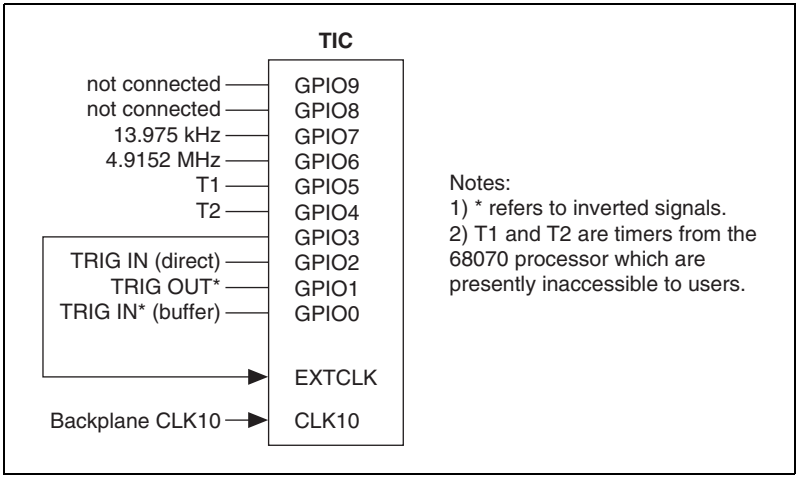


Figure F-1. GPIB-VXI/C GPIO Connections

G

Technical Support and Professional Services

Visit the following sections of the National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
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Glossary

Prefix	Meaning	Value
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

Symbols

°	degrees
Ω	ohms
%	percent

A

A	ampere

B

Backplane	an assembly, typically a printed circuit board, with 96 pin connectors and signal paths that bus the connector pins. VXIbus systems have either two sets of bused connectors, designated J1 and J2 backplanes, or three sets of bused connectors, designated J1, J2, and J3 backplanes.
BTO	Bus Timeout Unit
bytes/sec	bytes per second

C

C	Celsius
CI	*See* Code Instrument
Code Instrument	CI; a proprietary National Instruments software structure that uses software to emulate the capabilities of a VXI Message-Based device
Command	causes the GPIB-VXI/C to take some action
Commander	a Message-Based device that is also a bus master and can control one or more Servants
Console response	returned in the form of readable sentences, which is better suited for interactive command entry

D

DC	Dynamic Configuration, or Dynamically Configured
DC device	*See* Dynamic configuration device
DCI	*See* Downloaded CI
Diagnostics mode	mode in which you can perform extensive offline diagnostic tests of the GPIB-VXI/C
Downloaded CI	DCI; a form of CI that is downloaded into the GPIB-VXI/C's RAM memory
Dynamic configuration device	DC device; a device that initially has a logical address of 255. The RM subsequently assigns it a different, unique logical address

E

ECI	*See* EPROMed CI
EEPROM	Electrically Eraseable Programmable Read Only Memory

EPROM	Eraseable Programmable Read Only Memory
EPROMed CI	ECI; a form of CI that is user-installed into EPROMs

F

FIFO	First-In First-Out

G

GPIB	General Purpose Interface Bus. The industry standard IEEE 488 bus.
GPIB-VXI/C local command set	consists of commands and queries

H

Hz	Hertz (cycles per second)

I

IEEE	Institute of Electrical and Electronic Engineers
in.	inches

L

Logical address	an 8-bit number that uniquely identifies each VXIbus device in a system. It defines a device's A16 register address and indicates Commander/Servant relationships.
LSB	Least Significant Bit

M

m	meter
MB	megabytes of memory

Message-Based device	an intelligent device that implements the defined VXIbus registers and communication protocols
MODID lines	VXI backplane signals used by the Resource Manager (through the use of the Slot 0 device) in order to perform slot associations for logical addresses. There are 13 MODID lines, one for each slot in a full-size mainframe.
Module	typically consists of a board assembly and its associated mechanical parts, front panel, optional shields, and so on. A module contains everything required to occupy a slot in a mainframe. A module can occupy one or more slots.
MSB	Most Significant Bit

N

Nonvolatile configuration mode	mode in which you can edit the contents of the nonvolatile EEPROM memory
NV	nonvolatile memory

P

Peek	to read the contents
PH	Programmable Handler
PI	Position Independent
Poke	to write a value
pROBE	a low-level interactive debugger for use with the pSOS operating system. It is commercially available from Software Components Group, Inc. VXI pROBE is an enhanced version of pROBE supplied on developmental versions of the GPIB-VXI/C.
Program mode response	has a terse data-only format that is intended for a control program to read and parse
pSOS	a small, multitasking operating system kernel used on the GPIB-VXI/C. It is commercially available from Software Components Group, Inc.

Q

Query	similar to a command in that it also causes the GPIB-VXI/C to take some action, but it always returns a response containing data or other information

R

RCI	*See* Resident CI
Register-Based Device	a Servant-only device that supports VXIbus configuration registers. Register-Based devices are typically controlled by Message-Based devices via device-dependent register reads and writes.
Resident CI	RCI; a CI that is supplied by National Instrument and resides in the firmware
RM	*See* Resource Manager
Resource Manager	a Message-Based Commander located at Logical Address 0 that provides configuration management services such as address map configuration, Commander/Servant mappings, self-test and diagnostic management.

S

s	seconds
SC	Static Configuration, or Statically Configured
SC Device	*See* Static configuration device
Servant	a device that is controlled by a Commander. Any device can be a Servant.
Static configuration device	SC device; a device that has its logical address set by static means, such as by a DIP switch
System configuration table	during the execution of the RM and general configuration operations, the GPIB-VXI/C builds up a table of system configuration information. Each device has an entry in the table containing the device's logical address, its Commander's logical address, its secondary address, slot number, device class, manufacturer ID number, model code, memory space requirement, memory base address, and memory size. This table remains after the RM and general configuration operations are complete. It is accessible through the GPIB-VXI/C local command set.

V

V	volts
VME	Versa Module Eurocard or IEEE 1014
VXIbus	VMEbus Extensions for Instrumentation
VXI pROBE mode	mode in which you can use the enhanced pROBE debugger. This mode is available only with the GPIB-VXI/C development firmware option.
VXI system mode	the startup mode for normal operation in a VXI system

W

W	watts
Word Serial communication	the simplest form of communication required by Message-Based devices. It utilizes the A16 communication registers to transfer data using a simple polling handshake method.
Word Serial Protocol	the rules and regulations involved in performing Word Serial communication

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